Intel® 31154 133MHz PCI Bridge

Developer's Manual

January 2004

Order Number: 278848-001

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Revision History

Date	Revision	Description
January 2004	001	Initial Release.

Introduction 1

1.1 Product Overview

The Intel® 31154 133MHz PCI Bridge is a PCI component that functions as a highly concurrent, low latency transparent bridge between two PCI busses. The 31154 133MHz PCI Bridge is capable of operating as a PCI-to-PCI bridge in the configurations shown in Table 1.

Table 1. PCI-to-PCI Bridge Configurations

Primary Bus Interface	Secondary Bus Interface
PCI Local Bus Specification, Revision 2.3	*PCI Local Bus Specification*, Revision 2.3
PCI Local Bus Specification, Revision 2.3	*PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a
PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a	*PCI Local Bus Specification*, Revision 2.3
PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a	*PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a

The 31154 133MHz PCI Bridge is used on motherboards as a means of to provide additional I/O expansion slots. It is also used on PCI add-in cards as a means of mitigating the restrictive electrical loading constraints imposed on an expansion slot, enabling multiple conventional PCI or multiple PCI-X devices to reside on a single PCI I/O adapter.

The 31154 133MHz PCI Bridge has additional hardware support for Compact PCI Hot Swap and Redundant System Slot via queue flush, arbiter lock, and clock output tri-stating.

The 31154 133MHz PCI Bridge supports any combination of 32- and 64-bit data transfers on its primary and secondary bus interfaces. The bridge is 33/66 MHz capable in conventional PCI mode, and can run at 66 MHz, 100 MHz, or 133 MHz when operating in PCI-X mode depending upon its surrounding environment.

1.2 Features List

Table 2. Features List

- PCI Bus Interfaces (2):
  - — *PCI Local Bus Specification*, Revision 2.3 compliant.
  - — *PCI-to-PCI Bridge Architecture Specification*, Revision 1.1 compliant.
  - — *PCI Bus Power Management Interface Specification*, Revision 1.1 compliant.
  - — *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a compliant.
  - — External SROM support.
  - — Vital Products Data (VPD) Support.
  - — 64-bit Initiator/Target Capable.
  - — 64-bit addressing.
- Hardware Support for Dual Host CPCI Configurations.
- *Compact PCI Hot Swap Specification*, Revision 2.1 R2.0 Support.
- Secondary Clock generation with 10 clock outputs.
- Secondary Bus Arbitration:
  - — Internal Arbiter Supports nine agents in addition to 31154 133MHz PCI Bridge.
  - — Internal Arbiter can be disabled.
  - — Optimized for PCI-X mode.
  - — Bus parking on bridge or last master.
- Improved Buffer Architecture:
  - — 8 K Bytes Data Buffers in each direction.
  - — Improved level of Concurrency

    Up to nine outstanding transactions on each bus simultaneously.
- Scalability/ Flexibility:
  - — Conventional PCI 32/64-bit 33/66 MHz, 3.3 V,
  - — 5 V Tolerant inputs,
  - — PCI-X 32/64-bit 66/100/133 MHz, 3.3 V.
- JTAG interface.
- GPIO interface:
  - — Allows simple software-controlled signaling protocols.

1.3 Related External Specifications

- *PCI Local Bus Specification*, Revision 2.3.
- *PCI-to-PCI Bridge Architecture Specification*, Revision 1.1.
- *PCI Bus Power Management Interface Specification*, Revision 1.1.
- *Compact PCI Hot Swap Specification*, Revision 2.1 R2.0.
- *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.

Signal Descriptions 2

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type:

Ts Tri-State

Sts Sustained Tri-State

Od Open Drain

I Input pin

O Output pin

I/O Bi-directional Input/Output pin

2.1 PCI Bus Interfaces

Table 3. PCI Bus Interfaces (Sheet 1 of 3)

Signal	Width	Type	Description
P_AD[31:0]; S_AD[31:0]	32; 32	Ts-I/O	PCI Address/Data. These signals are a multiplexed address and data bus. During the address phase or phases of a transaction, the initiator drives a physical address on AD[31:0]. During the data phases of a transaction, the initiator drives write data, or the target drives read data.
P_CBE#[3:0]; S_CBE#[3:0]	4; 4	Ts-I/O	Bus Command and Byte Enables: These signals are a multiplexed command field and byte enable field. During the address phase or phases of a transaction, the initiator drives the transaction type on C/BE#[3:0]. When there are two address phases, the first address phase carries the dual address command and the second address phase carries transaction type. For both read and write transactions, the initiator drives byte enables on C/BE#[3:0] during the data phases.
P_PAR; S_PAR	1; 1	Ts-I/O	Parity: Even parity calculated on 36 bits - AD[31:0] plus C/BE[3:0]#. It is calculated on all 36 bits regardless of the valid byte enables. It is generated for address and data phases. It is driven identically to the AD[31:0] lines, except that it is delayed by exactly one PCI clock. PAR is an output during the address phase for all Intel® 31154 Bridge initiated transactions and all data phases when 31154 133MHz PCI Bridge is the initiator of a PCI write transaction.
P_DEVSEL#; S_DEVSEL#	1; 1	Sts-I/O	Device Select: As a target, 31154 133MHz PCI Bridge asserts DEVSEL# when a PCI master peripheral attempts an access to an internal address or the address of a resource that resides on 31154 133MHz PCI Bridge's other bus. As an initiator, DEVSEL# indicates the response to a 31154 133MHz PCI Bridge initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by 31154 133MHz PCI Bridge until driven as a target.

Table 3. PCI Bus Interfaces (Sheet 2 of 3)

Signal	Width	Type	Description
P_FRAME#; S_FRAME#	1; 1	Sts-I/O	Frame: FRAME# is driven by the Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated either the bus is idle, or is in the final data phase of the current bus transaction.
P_IRDY#; S_IRDY#	1; 1	Sts-I/O	Initiator Ready: IRDY# indicates the ability of the initiator to complete the current data phase of the transaction. A data phase is completed when both IRDY# and TRDY# are sampled asserted.
P_TRDY#; S_TRDY#	1; 1	Sts-I/O	Target Ready: Indicates the ability of the target to complete the current data phase of the transaction. A data phase is completed when both TRDY# and IRDY# are sampled asserted. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated by 31154 133MHz PCI Bridge until driven as a target.
P_STOP#; S_STOP#	1; 1	Sts-I/O	Stop: Indicates the target is requesting an initiator to stop the current transaction.
P_PERR#; S_PERR#	1; 1	Sts-I/O	Parity Error: Driven by an external PCI device when it receives data that has a parity error one PCI Clock following PAR/PAR64 signal assertion. Driven by 31154 133MHz PCI Bridge when, as an initiator, it detects a parity error during a read transaction as well as when receiving bad parity as the target of a write transaction.
P_SERR#	1	Od	Primary System Error: SERR# can be pulsed active by any PCI device that detects a system error including 31154 133MHz PCI Bridge.
S_SERR#	1	I	Secondary System Error: SERR# can be pulsed active by any PCI device that detects a system error condition except 31154 133MHz PCI Bridge. 31154 133MHz PCI Bridge samples SERR# as an input and conditionally forwards it to its primary interface.
P_REQ#	1	Ts-O	Primary Bus Request: 31154 133MHz PCI Bridge bus acquisition request input to the primary bus arbiter.
P_GNT#	1	I	Primary Bus Grant: Low assertion indicates that 31154 133MHz PCI Bridge is granted primary bus ownership following the completion of the current primary bus transaction.
S_REQ[8:1]#	8	I	Secondary PCI Requests: The internal arbiter supports up to nine external masters on the PCI bus using the S_REQ[8:1]# and S_REQ[0]# pins. See Section 4, “Arbitration” on page 69 for additional details.
S_REQ[0]#/ BR_GNT#	1	I	Secondary PCI REQ[0]# or Bridge GNT#: Depending upon whether or not the internal secondary arbiter is enabled, this signal serves as either a PCI request or a PCI grant. • When secondary arbiter is enabled this input represents S_REQ[0]#. • When secondary arbiter is disabled this input represents the 31154 133MHz PCI Bridge secondary bus master interface's PCI GNT#.
S_GNT[8:1]#	8	Ts-O	Secondary PCI Grants Supports up to nine other masters on the PCI bus. The arbiter can assert one of the nine bus grant outputs, to indicate that an initiator can start a transaction on the PCI Bus following completion of the current transaction.See Section 4, “Arbitration” on page 69 for additional details.

Table 3. PCI Bus Interfaces (Sheet 3 of 3)

Signal	Width	Type	Description
S_GNT[0]#/ BR_REQ#	1	TS-O	Secondary PCI GNT[0]# or Bridge REQ#: Depending upon whether or not the internal secondary arbiter is enabled, this signal serves as either a PCI request or a PCI grant. • When secondary arbiter is enabled this output represents S_GNT[0]#. • When secondary arbiter is disabled this output represents the 31154 133MHz PCI Bridge secondary bus master interface's PCI REQ#.
P_M66EN	1	I	Primary 66 MHz Enable: The Primary bus M66EN signal input is sampled on the trailing edge of P_RST#. This signal is used to determine the primary bus frequency when operating in conventional PCI mode. When sampled as 1b: Indicates that the primary bus interface will be operating in 66 MHz mode. When sampled as 0b: Indicates that the 31154 133MHz PCI Bridge primary bus interface will be operating in 33 MHz mode. **NOTE:** When the primary bus emerges from P_RST# in PCI-X mode the PCI-X initialization pattern that is broadcast by the Originating Device (host bridge typically) determine the primary bus frequency.
P_IDSEL	1	I	Primary ID SEL: This input serves as a high active chip select for Type 0 Configuration cycles that target the bridges configuration space registers.
S_M66EN	1	I	Secondary 66 MHz Enable: S_M66EN, along with S_PCIXCAP, indicate the mode (conventional PCI vs. PCI-X), and maximum frequency capabilities of the secondary bus devices.
S_PCIXCAP	1	I	Secondary PCI-X Capable: S_PCIXCAP, along with S_M66EN, indicate the mode (conventional PCI vs. PCI-X), and maximum frequency capabilities of the secondary bus.
Total	112		

2.2 PCI Bus Interface 64-Bit Extension (two interfaces)

Table 4. PCI Bus Interface 64-Bit Extension (two interfaces)

Signal	Width	Type	Description
P_AD[63::32]	32	Ts-I/O	PCI Address/Data: Multiplexed upper address and data bus. This bus provides an additional 32 bits to the PCI bus. During the data phases of a transaction, the initiator drives the upper 32 bits of 64-bit write data, and during 64 bit read transactions the target drives the upper 32 bits of 64-bit read data.When not driven AD[63:32] must be pulled up to a valid logic high level through external resistors.
S_AD[63::32]	32		
P_CBE#[7::4]	4	Ts-I/O	Bus Command and Byte enables upper 4 bits: These signals are a multiplexed command field and byte enable field. For both reads and write transactions, the initiator will drive byte enables for the AD[63:32] data bits on C/BE7:4] during the data phases when REQ64# and ACK64# are bothasserted.When not driven, C/BE#[7:4] is pulled up to a valid logic high level through external resistors.
S_CBE#[7::4]	4		
P_PAR64	1	Ts-I/O	PCI interface upper 32-bits parity: PAR64 carries the even parity of the 36 bits of AD[63:32] and C/BE#[7:4] for both address and data phases. When not driven, PAR64 is pulled up to a valid logic high level through an external resistor.
S_PAR64	1		
P_REQ64#	1	Sts-I/O	PCI interface request 64-bit transfer: REQ64# is asserted by the initiator to indicate that the initiator is requesting a 64-bit data transfer. It has the same timing as FRAME#. When 31154 133MHz PCI Bridge is the initiator, this signal is an output. When 31154 133MHz PCI Bridge is the target this signal is an input.
S_REQ64#	1		
P_ACK64#	1	Sts-I/O	PCI interface acknowledge 64-bit transfer: This is asserted by the target only when REQ64# is asserted by the initiator, to indicate the target ability to transfer data using 64 bits. It has the same timing as DEVSEL#.
S_ACK64#	1		
Total	78		

2.3 PCI Bus Interface Clocks and Reset

Table 5. PCI Bus Interface Clocks and Reset

Signal	Width	Type	Description
P_CLK	1	I	Primary PCI Clock Input
S_BRGCLKO	1	O	Secondary Bridge Clock Output: This output is identical to the other S_CLKO but does not have individual disable control. It is recommend for use as the feedback clock for the bridge and should be connected to S_CLKI. when the internal clock generation is used.
S_CLKO[8::0]	9	O	Secondary PCI Clock Outputs: 33/66/100/133 MHz clock for secondary bus PCI devices. These clocks can be disabled by strapping the S_CLKOEN[3:0] pins during reset. See Section 3.4.1.6, “Secondary Clock Control” on page 30 for additional details
S_CLKI	1	I	Secondary PCI Clock In: This signal is connected to an output of the low skew PCI clock buffer tree. When using the internal secondary clock generation, this pin should be connected to the S_BRGCLKO output.
S_CLKSTABLE	1	I	Secondary Clock Stable: This input is used to enforce the $T_{rst-clk}$ time as defined in the PCI Local Bus Specification. After this signal is asserted, the bridge will wait 100µS before deasserting the secondary PCI reset. When using internal secondary clock generation, this pin should be tied high.
S_GCLKOEN	1	I	Secondary Global Clock Output Enable: This pin should be pulled high to enable the secondary clock outputs. When deasserted (0b) all secondary clock outputs (S_CLKO[8::0] and S_BRGCLKO) will asynchronously tri-state. If an external clock source is used on the secondary interface, this signal should be pulled-low.
S_CLKOEN[3:0]	4	I (strap)	Secondary Clock Enable: These pins control the reset value of bits 8:0 in Section 5.2.4, “Offset 46H: VCR2 - 31154 Bridge Control Register 2”. The binary encoding on these pins indicates the number of secondary clock enabled.
P_RST#	1	I	Primary PCI Reset
S_RST#	1	O	Secondary PCI Reset: 31154 133MHz PCI Bridge asserts S_RST# to reset devices that reside on its secondary PCI bus. 31154 133MHz PCI Bridge asserts S_RST# due to one of the following events: • P_RST# assertion. • Setting the Secondary Bus Reset bit (bit 6) in the Bridge Control Register. • If PME# support from the $D3_{cold}$ is required, then a weak pull-down should be placed on the S_RST# line. This, in conjunction with PME# which is routed around the bridge, enables ACPI S3 (or higher) PME# operation for downstream PCI-PM compliant PCI agents.
Total	20		

2.4 JTAG

Table 6. JTAG

Signal	Width	Type	Description
TDI	1	I	Test Data In: TDI is the serial input through which JTAG instructions and test data enter the JTAG interface. TDI is sampled on the rising edge of TCK. If TDI is not driven, it produces the same results as if TDI were driven high.
TDO	1	O	Test Data Out: TDO is the serial output through which test instructions and data from the test logic leave 31154 133MHz PCI Bridge.
TMS	1	I	Test Mode Select: TMS causes state transitions in the test access port (TAP) controller. If TMS is not driven, it produces the same results as if TMS were driven high.
TCK	1	I	Test Clock: TCK is the clock controlling the JTAG logic. For systems that do not implement JTAG, this input should be pulled low.
TRST#	1	I	Test Reset: When TRST# is asserted (driven low), the TAP controller is asynchronously forced to enter a reset state, which in turn asynchronously initializes other test logic. TRST# must be pulled low to GND for normal operation.
SCAN_EN	1	I	SCAN Mode Select: The SCAN_EN pin toggles between the shift operation and the capture operation in the scan testing mode. It is used for scan chain testing of the device only. During normal operation, this input should be tied low.
TMODE[3:0]	4	I	Test Mode Select: These four pins are used to internally test 31154 133MHz PCI Bridge at the time of manufacture. TMODE3 must be tied to V_{SS} (logic 0) for normal operation. TMODE[2:0] all three pins must be tied to VSS (preferred) or all must be tied to V_{CC}. Normal Operation => 0000 or 0111.
MT#[1:0]	2	I	Manufacture Test pins. These two pins must be pulled high for normal operation.
Total	12		

2.5 Serial EEROM Interface

Table 7. Serial EEROM Interface

Signal	Width	Type	Description
SR_CLK	1	Ts-O	Serial EEROM Clock: Clock output. This pin is connected to the EEROM clock input.
SR_DI	1	Ts-O	Serial EEROM Data In: Serial data stream output that is connected to the EEROM DI input.
SR_DO	1	I	Serial EEROM Data out: Serial data stream input that is connected to the EEROMs DO output.
SR_CS	1	Ts-O	Serial EEROM chip select: 31154 133MHz PCI Bridge drives this signal high to enable the serial ROM for a read or write cycle.
Total	4		

2.6 CompactPCI Hot Swap

Table 8. Compact PCI Hot Swap

Signal	Width	Type	Description
HS_ENUM#	1	Od-O	Primary Bus Compact PCI Hot Swap Event: Conditionally asserted to notify the system host that either a board has been freshly inserted or is about to be extracted. This signal informs the system host that the configuration of the system has changed. The system host then performs any necessary maintenance such as installing or quiesing a device driver.
HS_LSTAT	1	I	Compact PCI Hot Swap Latch Status: An input to the bridge, indicating the state of the ejector switch. 0 = Indicates the ejector switch is closed. 1 = Indicates the ejector switch is open. If Compact PCI Hot Swap is not supported, this signal must be tied low.
HS_LED_OUT	1	O	LED Output: 31154 133MHz PCI Bridge outputs a logic one to illuminate the Hot Swap LED.
HS_SM	1	I	Hot swap Startup Mode: This pin is sampled at the rising edge of P_RST#. If 0b, 31154 133MHz PCI Bridge retries any Type 0 Configuration cycles addressed to it until it's serial ROM preload has completed. If 1b, 31154 133MHz PCI Bridge ignores (causes a master abort) any Type 0 configuration cycles address to it until it's serial ROM preload has completed. This pin should be tied low for non-Hot Swap systems.
HS_FREQ[1:0]	2	I	This pins are reserved for determining Primary Bus frequency and mode during a PCI-X hot swap event and are only valid when HS_SM = 1. The bus frequency and mode are described below: 00 => PCI Mode, 33 or 66 MHz. Use P_M66EN to determine frequency 01 => PCI-X Mode, 66 MHz 10 => PCI-X Mode, 100 MHz 11 => PCI-X Mode, 133 MHz These pins should be tied low for non-Hot Swap systems.
Total	6		

2.7 Hardware Straps

The values of the hardware strap pins specify the configuration options listed below. The values of these configuration options may be read from the Pre-boot Status device specific register, which is defined in Section 5.2.11, “Offset 56H: PB_STAT - Pre-Boot Status” on page 120.

Table 9. Hardware Strap / General Purpose I/O - Pins (GPIOS)

Signal	Width	Type	Description
S_ARB_DISABLE/ S_ARB_LOCK	1	I	Secondary Arbiter Disable / Arbiter Lock If sampled as 1b at the trailing edge of P_RST# the internal secondary bus arbiter is disabled. In this event S_GNT#[0) is used for the bridge’s secondary bus request output, and S_REQ#[0] is used for the bridge’s secondary bus grant input. If a logic low is sampled at the trailing edge of P_RST# then the bridge’s internal secondary arbiter is enabled for use. This pin must have either a pull-up resistor to V_{DD}, or a pull down resistor to Vss. It must no be left floating. If sampled as 1b after the trailing edge of P_RST# bridge’s internal secondary bus arbiter will lock and only provide the grant to itself.
S_MAX100	1	I (strap)	Secondary Bus Maximum Frequency: This trap bits, sampled on the trailing edge of P_RST#, provides 31154 133MHz PCI Bridge with necessary system specific secondary bus loading information that is required to correctly establish the maximum secondary bus clock frequency when operating in PCI-X mode. When asserted the secondary bus frequency will be limited to a maximum of 100 MHz. This pin must have either pull-up resistors to V_{DD}, or pull down resistors to Vss. It must not be left floating.
OPAQUE_EN	1	I (strap)	Opaque Memory Space Enable: If sampled high at the trailing edge of P_RST#, 31154 133MHz PCI Bridge will set bit 11 in the Section 5.2.4, “Offset 46H: VCR2 - 31154 Bridge Control Register 2” on page 110 which will enable the Opaque Memory Base/Limit registers. This establishes a private memory space for secondary bus usage, independent of the 31154 133MHz PCI Bridge downstream forwarding configuration.
IDSEL_MASK	1	I (strap)	IDSEL Masking Enable. If sampled high at the trailing edge of P_RST#, 31154 133MHz PCI Bridge will change the default value of the Section 5.2.13, “Offset 5CH: Secondary IDSEL Select Register - SISR” on page 122. Which will hide devices 16-21 from the host.
DEV_64BIT#	1	I (strap)	This signal is sampled on the trailing edge of P_RST# and sets bit 16 in the PCI-X Bridge Status Register. This strap is to support system management software and does not change the behavior to the bridge.
Total	5		

2.8 Miscellaneous

Table 10. Miscellaneous

Signal	Width	Type	Description
QE	1	O	Queues Empty: This output indicates the state of the 31154 133MHz PCI Bridge internal request and data queues. When at a logic high level this signal indicate that the 31154 133MHz PCI Bridge internal queues are completely empty. **NOTE:** State of this output is valid only when the NT_MASK# pin is asserted.
NT_MASK#	1	I	New Transaction Mask: When this pin is sampled asserted (logic low level), 31154 133MHz PCI Bridge does not enqueue any new transactions, except PCI configuration cycles targeting its configuration registers. Transactions enqueued at the time that this signal is sampled asserted are allowed to complete normally. Applications could for example, using this pin and the QE pin, implement external hardware that flushes 31154 133MHz PCI Bridge request and data queues.
S_TRISTATE	1	I	Secondary Bus Tri-State Enable: All Secondary bus outputs (except S_BRGCLKO) are asynchronously tri-stated when this signal is asserted(1b). In cPCI systems this input can be used to support Redundant System Slot (RSS) implementations. In non-RSS platforms, this pin should be tied directly to ground.
GPIO[7:0]	8	I/O	General Purpose I/O.
P_VIO	1	I	Primary Bus PCI Universal I/O Voltage Reference: This signal must be tied to either 3.3V or 5V, corresponding to the signaling environment of the primary PCI bus as described in the PCI Local Bus Specification. When any device on the primary bus uses 5V signaling levels, the system must connect P_VIO to 5V. P_VIO is connected to 3.3V by the system only when all the devices on the primary bus use 3.3V signaling levels.
S_VIO	1	I	Secondary Bus PCI Universal I/O Voltage Reference: This signal must be tied to either 3.3V or 5V, corresponding to the signaling environment of the secondary PCI bus as described in the PCI Local Bus Specification. When any device on the secondary bus uses 5V signaling levels, the system must connect S_VIO to 5V. S_VIO is connected to 3.3V by the system only when all the devices on the secondary bus use 3.3V signaling levels.
R_REF	1	I	R_REF: This pin is connected to an external (board-level) precision pull-down resistor. The resistor is used as a reference for setting the I/O buffers output drive AC and DC parametrics, enabling the output buffers to meet the PCI/PCI-X parametric specifications.
NC	2	O	No Connect: This output should be left floating.
RSRV[1:0]	2	I	Reserved: The reserved inputs should be pulled low to GND.
Total	17		

2.9 Total Signal Count

Total Signal Count

Interface	Signals
PCI Bus Interface	112
PCI 64-bit Extensions	78
Clock and Reset	20
JTAG	12
Serial ROM i/f	4
Compact PCI Hot Swap	6
Hardware Strap	5
Miscellaneous	17
Total	254

Bus Operation 3

This section details the operation of the Bus interfaces. Topics described in this section include:

- Reset
- Pre-Boot Component Initialization
- Bus Transactions
- Data Flow
- Conventional PCI operation
- PCI-X operation

3.1 RESET

The 31154 Bridge receives a primary bus reset input, P_RST#, and generates a secondary reset output, S_RST#. Additionally, the bridge supports a software controlled secondary bus reset mechanism defined by the PCI standard Secondary Bus Reset bit (Section 5.1.2, "Offset 04H: CMD - Command").

During P_RST# assertion, the internal state is completely initialized to its default state and the primary PCI bus data and control signals are tri-stated.

Setting the Bridge Control Register Secondary Reset Bit does not cause all of the internal state logic to be reset. However, all of the data queues, request queues, and associated control logic are re-initialized to their default state. The primary bus interface and all configuration space registers are not affected by setting the Secondary Reset Bit. Additionally, if there is a Serial ROM deployed, setting the Secondary Reset bit does not initiate a serial ROM pre-load sequence.

Note: A second configuration write is required to clear the Secondary Reset bit.

Table 11 outlines the reset mechanisms along with corresponding impact of each on the bridge. S_RST# is asserted for both reset mechanisms, but factors governing de-assertion of S_RST# and internal state reset varies between mechanisms.

Table 11. Reset Behavior Summary

Reset Mechanism	Full Component Reset?	Deassertion of S_RST#
P_RST#	Yes	S_RST# is asserted for a minimum of 100µS following the deassertion of P_RST# and the assertion of S_CLKSTABLE. Additionally, S_RST# will remain asserted until the completion of the serial ROM pre-load sequence (if serial ROM deployed).
Secondary Reset Bit set to 1b	No. Reset the secondary bus interface, data/request queues and associated state logic only.	On clearing of Secondary Reset bit via configuration write cycle to the bridge control register bit(6) Software must ensure that the required minimum reset time of 1mS is observed.

Note: A transition from the D3 hot state to the D0 device PM state will reset the required PCI header space but will not reset the device specific registers. SROM preload does not occur, and S_RST# is not asserted to the secondary bus.

3.2 Secondary Clock Stability

The bridge will ensure that S_RST# remains asserted for 100µS following the deassertion of P_RST# and the assertion of S_CLKSTABLE.

If an external clock source is used, then S_CLKSTABLE should be asserted once the clock source is stable at the desired frequency. The bridge is expecting a single transition to the asserted state and will sample S_CLKSTABLE after P_RST# deasserts. Future transitions of S_CLKSTABLE are ignored.

If the secondary clock source is guaranteed to be stable prior to P_RST# deassertion, or the internal secondary clock outputs are utilized, then S_CLKSTABLE may be pulled-up to V_{CC}.

3.3 Secondary Bus Central Resource

The 31154 Bridge always performs at least some of the Central Resource functions for it's secondary bus. As such, any time the secondary bus is in a reset state, (i.e., S_RST# is asserted), the secondary PCI bus is driven as described in Table 12.

Table 12. Secondary PCI Bus State During S_RST# Assertion

REQ64#	AD(63:32)	AD(31:0)	CBE(7:4)#	CBE(3:0)#	PAR64	PAR	PCI Control Signals
logic low	Hi-Z	logic low	Hi-Z	logic low	Hi-Z	logic low	Hi-Z

Note: If S_TRISTATE is asserted at any time (even during reset), the bridge will tristate all its Secondary PCI outputs, including reset, clocks, AD bus, and control signals.

While the 31154 Bridge always establishes a steady state 64-bit secondary bus when that bus is in the reset state, its internal secondary PCI Bus arbiter may be disabled if an external arbiter implementation is desired.

3.4 Pre-Boot Component Initialization

Through the use of strapping pins, and/or upon execution of an optional serial ROM pre-load, several of the 31154 Bridge features can be configured prior to host software initialization of the bridge. Key bridge secondary bus attributes that are configured prior to host involvement include:

- Internal Arbiter Enable/Disable.
- Maximum Allowable Secondary Bus Operating Frequency.
- Compact PCI Hot Swap Mode Select.
- Enable the Opaque Memory Region.

- Enable Secondary IDSEL Masking.
- Disable Secondary Clocks.

3.4.1 Pin Strap Configuration

The 31154 Bridge provides a number of inputs that must be strapped either high or low to configure the above features prior to host initialization of the bridge. All strapping options are sampled on the low-to-high, trailing edge of P_RST#.

Note: Some strap pins also perform some run time operations. These will be discussed where appropriate.

3.4.1.1 Secondary Arbiter Enable/Disable

The 31154 Bridge integrates a secondary bus arbiter which, in most operating environments, yields the optimum bridge performance. To support system or add-in adapter applications that wish to supply their own secondary bus arbiter a strapping option is provided to disable the internal arbiter.

The internal secondary bus arbiter is disabled when the ARB_DISABLE input is sampled as 1b at the trailing edge of P_RST#. If disabled the roles of the secondary REQ0# and GNT0# signals are reversed. The GNT0# output pin/signal now represents the bus REQ# into the external arbiter, and the REQ0# input to is used to indicate the bridge's GNT# from the external arbiter.

The ARB_DISABLE input is also used after reset to implement Arbiter Locking. If this pin is asserted after reset the bridge will lock the internal arbiter and only grant the bus to itself.

When used in conjunction with Queue Flushing, the ARB_DISABLE should only be asserted after the flush has completed.

Refer to Section 4, “Arbitration” on page 69 for detailed information on arbitration.

3.4.1.2 Secondary Bus Maximum Allowable Frequency

The 31154 Bridge supports secondary bus operation in either conventional PCI or PCI-X modes. As per the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a the secondary bus must be configured for mode as well as for operating frequency when coming out of S_RST#. The 31154 Bridge supports the S_MAX100 strapping pin to provide system information necessary to choose the correct operating speed for the bus. When MAX_100 is sampled as 1b at the trailing edge of P_RST#, the secondary bus is limited to a maximum of 100 MHz operation in PCI-X mode.

Refer to Section 3.4.4.2, “Secondary Bus Mode and Frequency Initialization” on page 39 for additional detail.

3.4.1.3 Compact PCI Hot Swap Mode Select

HS_SM must be asserted (1b) to enable Hot Swap functionality.

HS_FREQ[1:0] pins allow the bridge to determine the cPCI backplane operating frequency on its primary interface without needing to see a PCI-X initialization pattern. These pins are only valid when HS_SM is sampled as 1b during P_RST#.

Table 13. HS_FREQ Encoding

HS_FREQ[1:0]	P_M66EN	Operating Mode	Bus Frequency
00	0	PCI	33 MHz
00	1	PCI	66 MHz
01	-	PCI-X	66 MHz
10	-	PCI-X	100 MHz
11	-	PCI-X	133 MHz

3.4.1.4 Opaque Memory Region Enable

The 31154 Bridge supports an opaque memory region to enable private memory space for secondary devices. When OPAQUE_EN is sampled as 1b at the trailing edge of P_RST#, the Opaque Memory Enable bit in the Table 62, “VCR2 - 31154 Bridge Control Register 2” on page 110 will be set.

The default base and limit, reserved the upper half of memory (AD[63] = 1) for the private memory region.

3.4.1.5 Secondary IDSEL Masking

The 31154 Bridge supports private devices through the use of IDSEL Masking. If the IDSEL_MASK pin is sample as 1b on the trailing edge of P_RST# the default value for the Table 71, “Secondary IDSEL Select Register - SISR” on page 122 will be 001Fh to mask devices 0-4.

3.4.1.6 Secondary Clock Control

The 31154 Bridge provides the ability to disable its secondary clock outputs individually or globally. The straps S_CLKOEN[3:0] determine the number of S_CLKO[8:0] outputs that are enabled. The S_BRCLKO output is dedicated for the bridge feedback clock and cannot be individually disabled.

When the global clock output enable S_GCLKOEN is sampled as 0b all secondary clock outputs are disabled and an external clock source is required. 31154 Bridge will still drive the PCI-X initialization pattern, so any external clock source would have to be consistent with the bridges clock generation scheme defined in Section 3.4.4.2, “Secondary Bus Mode and Frequency Initialization” on page 39.

To support Redundant System Slot systems, the S_GCLKOEN input can also be used during runtime to synchronously tristate the secondary clock outputs. When S_GCLKOEN is sampled 0b, the 31154 Bridge will asynchronously tri-state all secondary clock outputs.

3.4.2 Serial ROM Interface

The 31154 Bridge provides a glueless interface to an optional 512-Byte serial EEPROM that may be used for loading the 31154 Bridge configuration space register settings prior to host system discovery and initialization of the bridge. The 31154 Bridge serial ROM interface is compatible with industry standard 512-Byte Microwire* serial ROM such as Microchip Technology, Inc., 93LC66A 512x8 serial EEPROM.

The clock input to the serial ROM is approximately 500 KHz and is established by dividing down the primary bus clock input (P_PCLK). The duty cycle is approximately 50%.

The format for the serial ROM data is detailed in Section 3.4.2.4, “Serial ROM Data Format” on page 36. The optional serial ROM also supports the Vital Product Data (VPD) interface as described in Section 3.4.3, “Vital Product Data” on page 38.

The serial ROM interface consists of four signals, as shown in Table 14. The serial ROM may be attached directly to the serial ROM pins without any additional external logic.

Table 14. Serial ROM Interface Signals

Name	Type	Description
SR_CS	O	Serial ROM Chip Select
SR_CLK	O	Serial ROM Clock
SR_DI	O	Serial ROM Data In
SR_DO	I	Serial ROM Data Out

3.4.2.1 Serial ROM Pre-Load Operation

The serial ROM interface and optional serial ROM are used to pre-load 31154 Bridge device-specific configuration registers, whenever the 31154 Bridge configuration registers are reset, due to the assertion of P_RST#.

Table 15 describes the two sequences that occur when emerging from secondary bus reset.

Table 15. Serial ROM Pre-Load Sequencing

P_RST#	S_RST#	SR_CS	Host Access to Bridge Configuration Space
Low	Low	Inactive	none
High	Low	Active (pre-load execution)	Retried if attempted[a]
High	High	Inactive (pre-load complete)	Accessible by host

a. If 31154 Bridge is configured for Compact PCI Hot Swap mode (HS_SM = 1), host access will be ignored resulting in a Master Abort on the primary interface.

The 31154 Bridge automatically executes a serial read from the ROM once P_RST# has gone inactive. S_RST# is de-asserted once the Serial ROM preload operation has completed. All 31154 Bridge initialization data is loaded with a single read operation by keeping the chip select asserted and toggling the clock. All throughout the Serial ROM pre-load process, The 31154 Bridge retries any configuration accesses until the pre-load sequence has completed. The pre-load sequence takes approximately 570 µsec. if P_PCLK is operating at 33 MHz (approximately 550 cycles * 1.08 µsec./cycle).

If the serial ROM is present, but a register pre-load is not desired, bits [7:6] of the first byte (the first two bits read) should read as any value except the pre-load enable value (i.e.,10b).

If the 31154 Bridge does not detect the pre-load enable two bit sequence, it stops the pre-load operation. In this case, all serial ROM pre-loadable configuration registers remain at their reset default values.

Note: If the optional Serial ROM is not deployed the VPD Capability List registers are made invisible to PCI bus scans.

3.4.2.2 Serial ROM Operation by Configuration Register Access

The 31154 Bridge allows serial ROM access through configuration register control. VPD registers or Serial ROM access registers are used to access external EEPROM. A serial ROM operation consists of the following three phases:

1. Command phase of three bits (first bit is a sync bit that is always a “1”).
2. Address phase of nine bits.
3. Data phase of eight or more bits.

Read/Write operations utilizing device specific SR_ADDR and SR_DATA programming interface, are executed as 32-bit data transfers, beginning on DWORD aligned address locations. Access to VPD area (080h and above) should only be made through VPD configuration registers (see Section 5.3.3, “Vital Products Data (VPD)” on page 143).

Accesses via serial ROM configuration registers are capable of reading and writing entire serial ROM. Read operations channel the data from the serial ROM to 31154 Bridge over the SR_DO signal. Write operations channel the data from the 31154 Bridge to the serial ROM over the SR_DI signal.

Table 16 and Table 17 are provided for completeness. The 31154 Bridge transparently handles all lower level signaling protocol, while the user is presented with a simple programming interface as described in the Section 3.4.2.2.1, “Executing a Serial ROM Read Transaction” on page 34 and Section 3.4.2.2.2, “Executing a Serial ROM Write Operation” on page 34.

Possible serial ROM transaction types and their opcodes are listed in the following tables.

Table 16. Serial ROM Transaction Opcodes

Opcode	Transaction	Opcode	Transaction
00	Write enable, write disable, write all, erase all	10	Read
01	Write	11	Erase

For Opcode 00, a byte address is not used, and the two most significant address bits [8:7] distinguish between the four commands:

Table 17. Opcode 00 Commands

AD[8:7]	Command	AD[8:7]	Command
00	write disable	10	Erase all
01	write all	11	write enable

The 31154 Bridge serial ROM interface supports the read, write, write enable, and write disable operations. Read and write operations are performed on demand using the VPD or Serial ROM Access register interfaces. The Write Enable signaling protocol is performed automatically before a serial ROM write, and a Write Disable signaling protocol is performed automatically after the serial ROM write.

The most significant bit written to the Serial ROM Address register determines direction of transfer:

- Writing the MSB of the Serial ROM Address register to 1b indicates a write operation.
- Writing the MSB of the Serial ROM Address register to 0b indicates a read operation.

Serial ROM Address Register MSB is toggled to opposite value when operation has completed. Read data can then be obtained by reading appropriate Data register[1], and next serial ROM operation can then be programmed. A write operation may take 10 ms or more to complete internal to ROM. A poll of the serial ROM is automatically performed to discover when a write operation completes.

3.4.2.2.1 Executing a Serial ROM Read Transaction

1. The initiator writes a DWORD aligned address into the Serial ROM Address register (SR_ADDR, offset 4Ah) with the MSB, (bit(15)), set = 0b. The address for the transaction is written into bits(8:2). All other bits in the register (bits(14:09;1:0)) are reserved and must be written all zeros.
2. Software now polls the SR_ADDR register looking for bit(15) to change state, (i.e., from 0b to 1b).
3. When bit(15) of the SR_ADDR register has changed state to 1b indicating “operation complete”, software may then retrieve the 32-bit read data from the Serial ROM Data register (SR_DATA, offset 4Ch).

3.4.2.2.2 Executing a Serial ROM Write Operation

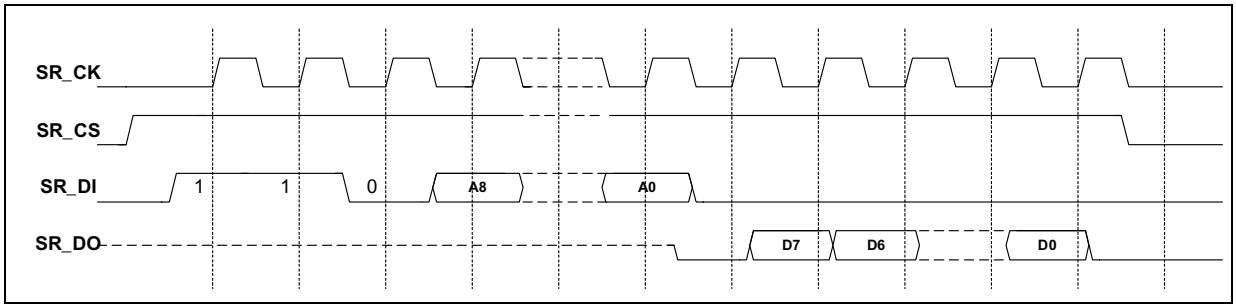
1. Software first writes a DWORD (4 bytes) of data into the SR_DATA register, bits(31:0).
2. Software then writes a DWORD aligned address into the SR_ADDR register with the MSB, (bit(15)), set = 1b. The address for the transaction is written into bits(8:2). All other bits in the register (bits(14:09;1:0)) are reserved and must be written to all zeros. Note that the act of writing to the SR_ADDR register starts the transaction over the Microwire interface.
3. Software now polls the SR_ADDR register looking for bit(15) to change state, (i.e., from 1b to 0b). When the SR_ADDR register's MSB is read back as a 0b, the write is complete and the next serial ROM operation may be initiated.

3.4.2.3 Serial ROM Microwire Interface Signaling Protocol

Figure 1 through Figure 5 show the timing diagrams for serial ROM read, write, write enable, write disable, and check status (polling) operations.

Note: Serial ROM access using the VPD or Serial ROM access mechanism should not be attempted if a serial ROM is not deployed as undefined behavior may result.

Figure 1. Serial ROM Read Timing Diagram



1. Either from the VPD Data register, or from the Serial ROM Data register depending upon the access method used for the transaction.

Figure 2. Serial ROM Write Timing Diagram

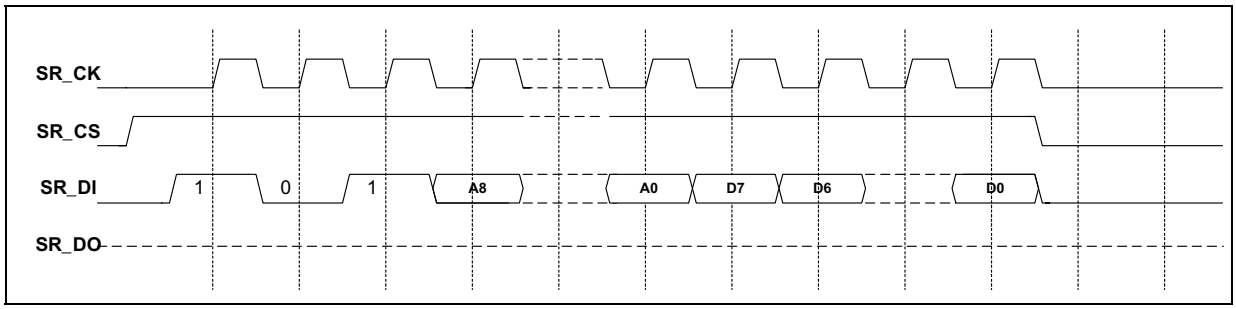


Figure 3. Serial ROM Write Enable Timing Diagram

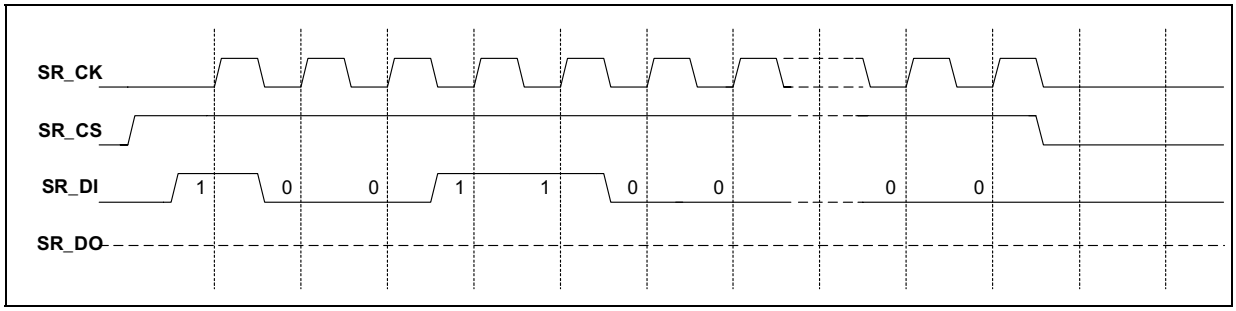


Figure 4. Serial ROM Write Disable Timing Diagram

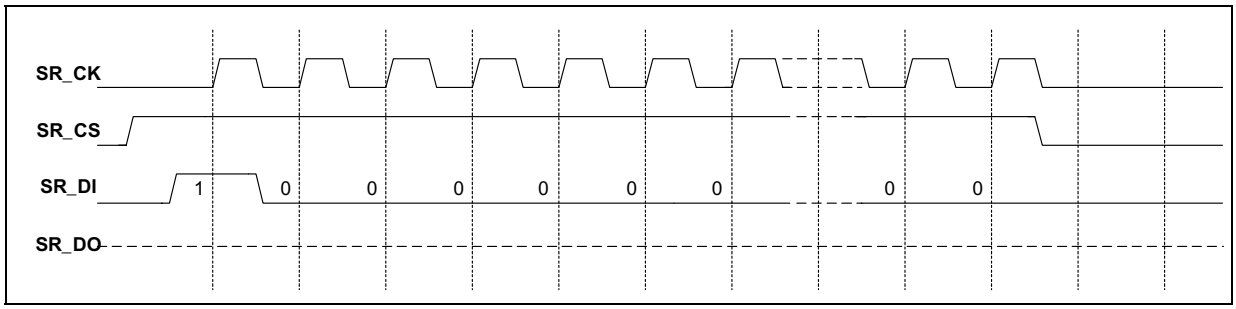
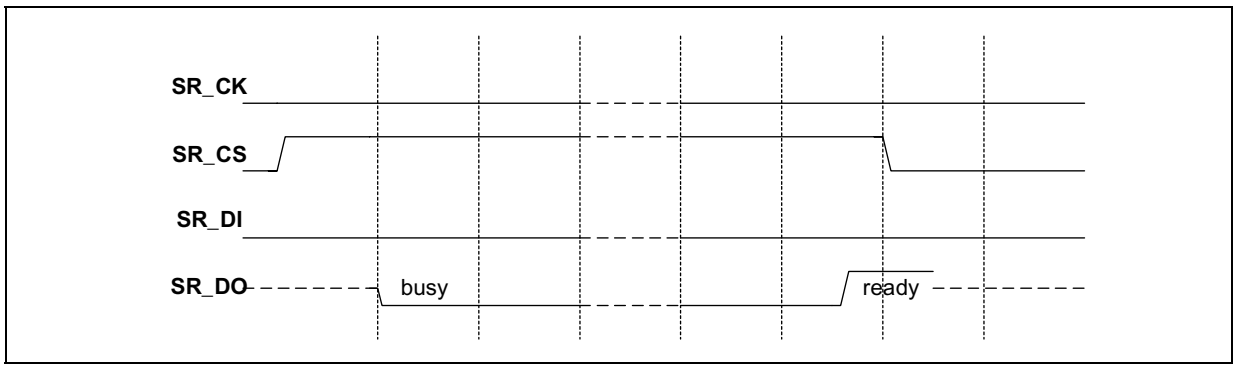


Figure 5. Serial ROM Check Status Timing Diagram



3.4.2.4 Serial ROM Data Format

Table 18 details the layout of the Serial ROM. Note that only a subset of the 31154 Bridge internal registers are Serial ROM pre-loadable.

Reserved or unused bits must be written to 0b when formatting the Serial ROM contents.

Table 18. Serial Pre-Load Sequence (Sheet 1 of 2)

Byte offset	Description
00h	[7:6] 10 to enable serial pre-load [5:1] 00000 Reserved [0] 1 load Vendor ID/Device ID/Revision ID [0] 0 do not load Vendor ID/Device ID/Revision ID.
01h	Arbiter Control / Status[7:0]
02h	Arbiter Control / Status[15:8]
03h	31154 Bridge Control Register 0
04h	31154 Bridge Control Register 1[7:0]
05h	31154 Bridge Control Register 1[15:8]
06h	31154 Bridge Control Register 2[7:0]
07h	31154 Bridge Control Register 2[15:8]
08h	Multi-Transaction Timer Register[7:0]
09h	Multi-Transaction Timer Register[15:8]
0Ah	Pre-Fetch Policy Register[7:0]
0Bh	Pre-Fetch Policy Register[15:8]
0Ch	P_SERR# Assertion Control Register[7:0]
0Dh	P_SERR# Assertion Control Register[15:8]
0Eh	Secondary IDSEL Select Register[7:0]
0Fh	Secondary IDSEL Select Register[15:8]
10h	Secondary IDSEL Fnct 0 Enable Register[7:0]
11h	Secondary IDSEL Fnct 0 Enable Register[15:8]
12h	GPIO Pin Configuration Register
13h	GPIO Write One to Toggle Register
14h	Opaque Memory Base and Limit Register[7:0]
15h	Opaque Memory Base and Limit Register[15:8]
16h	Opaque Memory Base and Limit Register[23:16]
17h	Opaque Memory Base and Limit Register[31:24]
18h	Opaque Memory Base Upper 32 Bits[7:0]
19h	Opaque Memory Base Upper 32 Bits[15:8]
1Ah	Opaque Memory Base Upper 32 Bits[23:16]
1Bh	Opaque Memory Base Upper 32 Bits[31:24]
1Ch	Opaque Memory Limit Upper 32 Bits[7:0]
1Dh	Opaque Memory Limit Upper 32 Bits[15:8]
1Eh	Opaque Memory Limit Upper 32 Bits[23:16]
1Fh	Opaque Memory Limit Upper 32 Bits[31:24]
20h	Slot Number Register
21h	Chassis Number Register

Table 18. Serial Pre-Load Sequence (Sheet 2 of 2)

Byte offset	Description
22h	Power Management Next Item Pointer: Must be pre-loaded with a value of E4h to expose VPD register block to software.
23h	Power Management Capabilities Register[15:8] This register may be pre-loaded with high order bits [15:11] set to 11111b indicating that the bridge supports PME# generation from any PM DState. This feature may be used to workaround a Windows 98 bridge power management errata.
24h	ID [7:0] The Device ID and Vendor ID are only preloaded if SROM offset 00h = 1000_0001. Otherwise, offsets 24h-28h are ignored.
25h	ID [15:8].
26h	ID [23:16].
27h	ID [31:24].
28	RID The Revision ID is only preloaded if SROM offset 00h = 1000_0001. Otherwise, offsets 24h-28h are ignored.
29h - 7Fh	Reserved.
80h - 0FFh	Vital Product Data (Read Only region).
100h - 1FFh	Vital Product Data (Read / Write region).

3.4.3 Vital Product Data

The Vital Product Data (VPD) capability mechanism is supported through the serial ROM interface.

VPD is stored in the last 3 Kbits (384 bytes) of the serial ROM. The first 1 Kbits (128 bytes) of the VPD space are designated as read only and cannot be written from the VPD serial ROM register interface. The upper 2 Kbits (256 bytes) are designated as read/write from the VPD serial ROM register interface. Only VPD data can be accessed through this interface.

All VPD accesses reference DWORD aligned address locations, and are executed as 32-bit data transfers.

3.4.3.1 Reading VPD Information

Any location within VPD space can be read. Valid VPD byte addresses are 17F:000h. In order to read VPD information from the serial ROM, the following steps must be taken:

1. The VPD address and VPD Flag bits are written. This requires a write to bytes E7:E6h, where the low order bits carry the VPD address and bit 15 is set=0b, indicating a read operation. 31154 Bridge adds the VPD base address, 080h, to the VPD DWORD aligned address resulting in the serial ROM physical address and performs a read of 4 bytes.
2. Software then polls the VPD Flag bit (VPD Address register bit(15)). When 31154 Bridge returns a 1b, the read is complete and the data is available for retrieval in the VPD Data register.
3. The VPD read data is now retrieved via the VPD Data register. Byte 0 is the least significant byte, followed by Bytes 1:3 in order of increasing significance.

The VPD Address and VPD Data registers should not be written while a VPD read operation is currently in process.

3.4.3.2 Writing VPD Information

Only the last 2 Kb (256 bytes) of VPD Space can be written using the VPD programming interface. (17C:080h). The following steps must be taken to write VPD information into the serial ROM:

1. The VPD data register is written with four bytes of data.
2. The VPD address and VPD Flag bits are written. This requires a write to bytes E7:E6h, where the low order bits carry the VPD DWORD aligned address and bit 15 is a 1b, indicating a write operation. 31154 Bridge adds the VPD base address, 080h, to the VPD DWORD aligned address resulting in the serial ROM physical address and performs a write of four bytes.
3. The VPD Flag bit is polled. When The 31154 Bridge returns a 0b, the write is complete.

If a write is attempted to a location in the first 1Kbits of serial ROM space (address bits (8:7) = 00b), the 31154 Bridge does not perform the write operation and clears the VPD flag bit immediately.

The VPD Address and VPD Data registers should not be written while a VPD write operation is taking place.

3.4.4 Bus Mode and Frequency Initialization

Both of the PCI bus interfaces are capable of operating at a variety of frequencies, and in either conventional PCI mode, or in PCI-X mode. Each interface establishes the bus mode and frequency when coming out of its corresponding bus segment reset sequence. The resultant mode and frequency is dependent upon the device capabilities reported as well as any system specific loading information.

3.4.4.1 Primary Bus Mode and Frequency Initialization

The 31154 Bridge reports its primary bus operating capabilities to the primary bus segments originating device (typically the host bridge). The 31154 Bridge indicates to the primary bus segments originating device that its primary interface is PCI-X capable at frequencies of up to 133 MHz inclusive. It also indicates that the 31154 Bridge is capable of running at 66 MHz when operating in conventional PCI mode.

3.4.4.2 Secondary Bus Mode and Frequency Initialization

The 31154 Bridge is the originating device for its secondary bus, and as such sets the bus mode and frequency when exiting out of the secondary bus reset sequence. The two key components that factor into the resultant secondary bus mode and frequency are the PCI-X standard sampling of downstream device capabilities, and the system specific physical bus loading characteristics for which the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a does not provide any standard means of reporting.

Downstream device capabilities are indicated by the values of S_M66EN, and S_PCIXCAP during S_RST# assertion.

Table 19. Device Mode/Frequency Capability Reporting

M66EN	PCIXCAP	Convention PCI Device Frequency Capability	PCI-X Device Frequency Capability
Ground	Ground	33 MHz	Not capable
Not connected	Ground	66 MHz	Not capable
Ground	Pull-down	33 MHz	PCI-X 66 MHz
Not connected	Pull-down	66 MHz	PCI-X 66 MHz
Ground	Not connected	33 MHz	PCI-X 133 MHz
Not connected	Not connected	66 MHz	PCI-X 133 MHz

Note: Knowledge of the device capabilities alone is insufficient information to robustly select the bus frequency. In order to be sure of what the bus operating frequency should be set to, knowledge of the bus layout (e.g., number of slots), is also necessary.

If, for example, a 133 MHz PCI-X capable adapter was the sole occupant of a two slot segment, then it would be necessary to slow the bus to 100 MHz, even though the card reported it could operate at 133 MHz due to the additional electrical loading imposed by the two slot board and connector layout.

The 31154 Bridge provides the S_MAX100 strapping pin for reporting system specific secondary bus loading information that is used in determining the maximum operating frequency of the secondary bus. The 31154 Bridge considers S_MAX100 along with S_PCIXCAP and S_M66EN# to determine the secondary bus mode and frequency when emerging from S_RST#.

- To limit the bus to conventional PCI mode, ground the PCIXCAP pin on the system board.
- To limit the bus to 33 MHz conventional PCI, ground the S_M66EN on the system board.

- To limit the bus to 66 MHz PCI-X, add a pull-down and capacitor to the system board as described in section 9.10 of the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.

Table 20 details the secondary bus frequency initialization as a function of S_MAX100, and the sampled secondary device capabilities.

Table 20. Secondary Bus Frequency Initialization

M66EN	PCIXCAP	S_MAX100	Conventional PCI Frequency	PCI-X Frequency	Typical Slot Loading
Ground	Ground	-	33 MHz	Not capable	
Not Connected	Ground	-	66 MHz	Not capable	
Ground	Pull-down	-	33 MHz	PCI-X 66 MHz	Typical setting for 4 slots
Not Connected	Pull-down	-	66 MHz	PCI-X 66 MHz	
Ground	Not Connected	1	33 MHz	PCI-X 100 MHz	
Not Connected	Not Connected	1	66 MHz	PCI-X 100 MHz	Typical setting for 2 slots
Ground	Not Connected	0	33 MHz	PCI-X 133 MHz	
Not Connected	Not Connected	0	66 MHz	PCI-X 133 MHz	Typical setting for 1 slot

Table 21 describes the bus mode and frequency initialization pattern that the 31154 Bridge signals on its secondary bus when coming out of S_RST#, after having evaluated the above information.

Table 21. PCI-X Initialization Pattern

DEVSEL#	STOP#	TRDY#	Mode	Clock Period (Ns)		Clock Frequency (MHz)	
				Max	Min	Min	Max
Deasserted	Deasserted	Deasserted	PCI 33	¥[a]	30	¥	33
			PCI 66	30	15	33	66
Deasserted	Deasserted	Asserted	PCI-X	20	15	50	66
Deasserted	Asserted	Deasserted	PCI-X	15	10	66	100
Deasserted	Asserted	Asserted	PCI-X	10	7.5	100	133
Asserted	Deasserted	Deasserted	PCI-X	Reserved			
Asserted	Deasserted	Asserted	PCI-X				
Asserted	Asserted	Deasserted	PCI-X				
Asserted	Asserted	Asserted	PCI-X				

a. When the internal PLLs are operational, the minimum input frequency is 16 MHz. See "Primary-to-Secondary Frequency Limits" on page 41 for more information.

Note: In early stages of PCI-X development, it is anticipated many add-in card manufacturers may have difficulty achieving fully compliant 133 MHz operation with designs utilizing currently available "off the shelf" ASIC process technology. The Secondary Bus Maximum Frequency strapping feature enables these devices to operate at 100 MHz even with no standard provisions in the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a for reporting device capability of 100 MHz operation.

If a card is plugged into a four slot secondary bus, grounding the M66EN and pulling-down the PCIXCAP ensures that the bus will run at no greater than 66 MHz in PCI-X mode, and no greater than 33 MHz in conventional PCI mode regardless of the reported downstream device capabilities.

If a card is plugged into a two slot secondary bus, the S_MAX100 strapping of 1b ensures that the bus will run at no greater than 100 MHz, regardless of the reported downstream device capabilities.

Finally, if a card is plugged into a single slot secondary (i.e., a segment that should be able to run at 133 MHz), by strapping the S_MAX100 bit to 1b (as though it were a two slot configuration), the bus will operate at 100 MHz maximum[1].

3.4.4.3 Primary-to-Secondary Frequency Limits

When operating in PCI 33 MHz mode the bridge will bypass the PLL to allow the full range of 0-33 MHz operations define in the PCI Specifications.

However, the PLL is used to generate the secondary clock outputs when the secondary side is operating at greater than 33 MHz (PCI-66 MHz or PCI-X). The primary clock input must operate above 25 MHz to ensure that the secondary frequencies are within the ranges defined in the PCI specifications.

If both primary and secondary sides are operating in PCI-33 MHz mode then the secondary clock will equal the primary clock in frequency.

An external clock source can be used on the secondary interface to remove any dependencies on the primary clock input.

1. Adapters that report 133 MHz PCI-X device capability with this MaxFreq setting will be limited to 100 MHz operation.

3.4.5 Private Devices on the Secondary Interface

Private devices are hidden from the host PCI configuration software. An intelligent agent on the secondary bus could still configure these private devices via Type 0 Configuration transaction on Secondary bus interface. To include private devices on the secondary interface, the bridge must be configured properly prior to system initialization.

To configure the bridge to support private devices, the user must:

- Mask secondary devices by utilizing the Table 71, "Secondary IDSEL Select Register - SISR" on page 122 or the IDSEL_MASK hardware strap.
- Enable the Private Memory Window utilizing the Opaque Memory Base and Limit Registers or OPAQUE_EN hardware strap.

3.4.5.1 Private Type 0 Commands on Secondary Interface

The 31154 Bridge will not claim Type 0 configuration reads and write commands on the Secondary bus interface. These Type 0 configuration commands are required to configure private PCI devices on the Secondary bus which are in private PCI address space. These commands are initiated by a external agent on the secondary bus and not by Type 1 commands on the Primary bus. Any device mapped into this private address space *will not* be part of the standard Secondary PCI address space and therefore will not be configured by the system host processor. These devices are hidden from PCI configuration software.

In Type 0 commands on the Secondary interface, **S_AD[31:11]** are used to select the **IDSEL** input of the target device. In Type 1 to Type 0 conversions, **P_AD[15:11]** are decoded to assert a unique address line from **S_AD[31:16]** on the Secondary interface.

The Secondary IDSEL Select Register (SISR) can be programmed to block 10 address lines during Type 1 to Type 0 conversions from the Primary interface. Secondary address bits **S_AD[25:16]** are the address lines that can be masked by the SISR register. By setting bits 0 through 9 (corresponding to **S_AD[16] - S_AD[25]**) in the SISR, the associated address line can be forced to remain deasserted for the **P_AD[15:11]** encodings of 00000_2 - 01001_2 and therefore are free to be used as an **IDSEL** select line for private Secondary PCI devices. Table 22 shows the possible configurations of **S_AD[31:11]** for public/private Type 0 commands on the Secondary interface. For example, if SISR Bit 0 is set, **S_AD[16]** will never be asserted during a Type 1 to Type 0 conversion from the Primary PCI bus. It can only be asserted by the Secondary Address Translation Unit.

Table 22. Public/Private PCI Memory IDSEL Select Configurations

Primary Address P_AD[15:11]	Secondary Addresses S_AD[31:11] with All SISR Bits = 0	Secondary IDSEL Select Register Bits 9-0[a]	Secondary Addresses S_AD[31:11] with SISR Bits Programmed
00000	0000 0000 0000 0001 0000 0_2	XXXXXXXXX1_2	0000 0000 0000 0000 0000 0_2
00001	0000 0000 0000 0010 0000 0_2	XXXXXXXX$1X_2$	0000 0000 0000 0000 0000 0_2
00010	0000 0000 0000 0100 0000 0_2	XXXXXXX$1XX_2$	0000 0000 0000 0000 0000 0_2
00011	0000 0000 0000 1000 0000 0_2	XXXXXX$1XXX_2$	0000 0000 0000 0000 0000 0_2
00100	0000 0000 0001 0000 0000 0_2	XXXXX$1XXXX_2$	0000 0000 0000 0000 0000 0_2
00101	0000 0000 0010 0000 0000 0_2	XXXX$1XXXXX_2$	0000 0000 0000 0000 0000 0_2
00110	0000 0000 0100 0000 0000 0_2	XXX$1XXXXXX_2$	0000 0000 0000 0000 0000 0_2
00111	0000 0000 1000 0000 0000 0_2	XX$1XXXXXXX_2$	0000 0000 0000 0000 0000 0_2
01000_2	0000 0001 0000 0000 0000 0_2	X$1XXXXXXXX_2$	0000 0000 0000 0000 0000 0_2
01001_2	0000 0010 0000 0000 0000 0_2	1$XXXXXXXXX_2$	0000 0000 0000 0000 0000 0_2

X = Don't Care

a. If the corresponding Secondary IDSEL Function 0 Enable Register Bit is set, the corresponding address bit will be unmasked for function 0 (P_AD[10:8] must equal 000_2).

The Secondary IDSEL Function 0 Enable Register (SIF0ER) may be used to assert an address line masked by the SISR for the Type 1 to Type 0 conversion associated with function 0 (**P_AD[10:8]** must equal 000_2). For multi-function PCI devices on the secondary bus, this capability would allow function 0 to remain public while functions 1-7 remain private (masked by the SISR). For example, if SISR Bit 0 is set and SIF0ER Bit 0 is set, **S_AD[16]** will be asserted for function number 0 and not be asserted for function numbers 1-7 during a Type 1 to Type 0 conversion from the Primary PCI bus.

If the Primary interface receives a Type 1 command that intends to use one of the **S_AD** address lines reserved for private PCI devices, the bridge will perform the Type 1 to Type 0 conversion but not assert the reserved **S_AD** address line. The Type 0 command will then be ignored on the Secondary PCI bus.

By using the SISR register, a total of 10 **IDSEL** signals are available for private PCI devices.

3.4.5.2 Private Memory Space

When Private Memory Space Enable in the VCR2 (Section 5.2.3, “Offset 44H: VCR1 - 31154 Bridge Control Register 1” on page 108) is set, the bridge will utilize the Opaque Memory Base and Limit Register and not forward upstream any secondary bus initiated Memory transactions within the Private Memory Range. This establishes a private memory space for secondary bus usage, independent of bridge downstream forwarding configuration.

See the Table 76, “OMBL - Opaque Memory Base and Limit Register” on page 129 for more details.

3.5 Device Select Timing

Targets are required to claim transactions by asserting DEVSEL# as shown in Table 23. The 31154 Bridge responds as a type A target (PCI-X), or Medium (conventional PCI).

Table 23. DEVSEL# Timing

Decode Speed	conventional PCI	PCI-X
1 clock after address phase(s)	Fast	Not Supported
2 clocks after address phase(s)	Medium	Decode A
3 clocks after address phase(s)	Slow	Decode B
4 clocks after address phase(s)	Subtractive	Decode C
5 clocks after address phase(s)	N/A	N/A
6 clocks after address phase(s)	N/A	Subtractive

3.6 64-Bit Operation

The 31154 Bridge is 64-bit capable on both of its bus interfaces. Primary and secondary bus interfaces can operate in any combination of 32- or 64-bit operation at any given time.

- As an initiator the bridge will asserts REQ64# when possible. Some exceptions are detailed below:Any DWORD transaction.
- When starting address is not QWORD aligned (conventional PCI mode only).
- When the total transaction length is less than four QWORDs.

As a target, the bridge asserts ACK64# in response an initiator's assertion of REQ64# with the following exceptions:

- Upstream Memory Read.
- Downstream MRL, MRM, or Memory Read to a non-prefetchable address space.
- Memory Read (MR, MRL, MRM) reconnection (because delayed read) which executed as a DWORD transaction on the destination bus.
- Any DWORD transaction.
- When the bus is configured to 32-bit mode during reset.
- When responding with a Split Response.

3.7 PCI Power Management Support

The 31154 Bridge is compliant with *PCI Bus Power Management Interface Specification*, Revision 1.1.

Following are some the 31154 Bridge PCI-PM specifics:

- Value in PMCSR[1:0] PowerState field dictates the 31154 Bridge ability to respond to and initiate transactions:

  00 - (D0 state) the 31154 Bridge responds to, and initiates transactions normally.

  01, 11 - the 31154 Bridge responds ONLY to type 0 configuration accesses. Does NOT master any transactions.

  10 - (D2 state) the 31154 Bridge does not implement the D2 state.

- When the PMCSR[1:0] is written to 00 from 11, an internal reset is performed transitioning the 31154 Bridge to the $D0_{uninitialized}$ state. Only the standard PCI Configuration registers are reset. All device specific registers retain their previous value. Additionally, the Serial ROM preload does not occur.

3.8 Flush Buffers Feature

The 31154 Bridge enables either software, or external hardware[1] to force the retirement or immediate invalidation of its internal request queues and data buffers, while disabling acceptance of any new transactions.

One possible usage for the invalidation feature is in support of Redundant System Slot (RSS) Compact PCI platform implementations, where the 31154 Bridge is deployed on an I/O peripheral controller card.

3.8.1 When Using the Programming Interface

3.8.1.1 To Flush the Queues

1. Set the New Transactions Mask (NT_MASK) bit to1b (in VCR0).
2. Poll the Queues Empty (QE) bit in VCR0. Once set this indicates that all internal queues are empty, and no new transactions are being accepted/enqueued until the NT_MASK bit is cleared to 0b.

3.8.1.2 To Invalidate the Queues

1. Set the Invalidate bit to 1b (in VCR0). This has the affect of both shutting off the acceptance of any new transactions, while also invalidating all request, and data queue entries.
2. Poll the Invalidate Complete bit to determine when the invalidation operation has completed. Only after having sampled a completed invalidation operation should the Invalidate bit be cleared to 0b enabling normal operation once again.

1. The hardware (pin) interface can only be used to flush the queues. Queue invalidation may only be performed using the software interface.

3.8.2 When Using the Hardware (Pin) Interface

3.8.2.1 To Flush the Queues

1. Assert the NT_MASK# pin.
2. Sample QE. If QE is asserted, NT_MASK operation was successful and queues are empty. Typically, if QE has not asserted after 10 µSec.[1], the application should assume an error condition had prevented bridge from flushing its queues.

Warning: Once the NT_MASK pin is asserted, it should not be deasserted until the QE pin is asserted. Likewise NT_MASK should not be reasserted until QE pin is cleared. If NT_MASK is toggled in any other fashion, the state of the QE pin is unreliable.

3.8.3 Returning to Normal Operation

3.8.3.1 Subsequent to Flushing the Queues

1. If QE never asserted (bit or pin), only way to return to normal operation is by asserting P_RST#. (This case would be indicative of a fatal error condition somewhere in the system)
2. If QE was asserted (successful queue flush), the application can then return the 31154 Bridge to normal operation by either clearing the NT_MASK bit to 0b, or de-asserting the NT_MASK pin, depending on whether the feature was invoked by the software, or hardware interface.

3.8.3.2 Subsequent to Invalidating the Queues

After having sampled the assertion of the Invalidate Complete bit, clear the Invalidate bit to 0b. Once the Invalidate bit is cleared the 31154 Bridge resumes normal operation.

1. Some applications may require additional time for full retirement of data.

3.9 General Purpose I/O Interface

The 31154 Bridge implements a 8-pin general-purpose I/O GPIO interface (GPIO(7:0)). The GPIO signals are managed by writing and reading into device-specific PCI configuration registers.

3.9.1 GPIO Control Registers

GPIO functionality is managed by programming the following three device-specific configuration registers:

- Pin Configuration register.
- Output Data “Write 1 to Toggle” register.
- Pin Status register.

All three of these device specific PCI configuration registers conform to the following bit assignments.

Table 24. GPIO Configuration Register Bit Assignments

Bit(7)	Bit(6)	Bit(5)	Bit(4)	Bit(3)	Bit(2)	Bit(1)	Bit(0)
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

3.9.1.1 Pin Configuration Register

The Pin Configuration register determines whether each corresponding GPIO is configured as input only or as a read/write output. Each GPIO bit is controlled independently by its corresponding bit in this register.

A given GPIO pin is configured as “Input Only” when its corresponding bit is set to 0b. Conversely, setting a given bit to 1b configures the corresponding GPIO as a read/write output pin.

3.9.1.2 Output Data “Write 1 to Toggle” Register

The 31154 Bridge provides a read/write 8-bit register for controlling the GPIO output states.

Writing a 1b to a given bit in this register causes its corresponding GPIO output pin to change state.

This mechanism for toggling the output state of individual GPIOs eliminates the need for software to comprehend and maintain the current state of any other GPIOs; other than those state(s) being toggled during any given write operation to this register.

This register may be read by software at any time. The value returned when reading this register corresponds to the current logic output levels for each of the GPIOs had they been configured as outputs; not to be confused with the actual state of the GPIO pins. The actual state of the GPIO pins can be observed by reading the Pin Status register. (described in the next section)

Writing 1b to any bit whose corresponding GPIO is configured for input has no direct affect on that particular pin. However when initializing the 31154 Bridge , the initial output state for a given GPIO pin could be established by performing the following sequence:

1. Establish the desired initial output state (high or low) of a given GPIO by writing the appropriate value into this register.
2. Writing the Pin Configuration register to then configure that particular GPIO as an output. (the Pin Configuration register's power up default state configures all GPIOs as inputs)

3.9.1.3 Pin Status Register

This 8-bit read only register returns the current status for all of the GPIO pins. Specifically, reads return the currently sampled states of all GPI pins as well as the states for what is currently being driven states on all GPO pins.

3.10 Overview of Bus Transactions

The following sub-sections detail bridge behavior when operating in conventional PCI/X modes.

For purposes of the following discussion the terms in Table 25 define the buses being described. Split Completions are the only transactions that arbitrate for and start on the Destination Bus.

Table 25. Bus Terms Description

Term	Description
Origination Bus	The bus which initiates a request. Bus closest to the Requester.
Destination Bus	The bus where a request is completed. Bus closest to the Completer. All Split Completion originate from this bus in response to a request that had been made on the Origination Bus.
PMW	Posted Memory Write.
NPMW	NOT (PMW).

Transaction crossing the bridge assume one of the following configurations:

- PCI to PCI.
- PCI-X to PCI.
- PCI to PCI-X.
- PCI-X to PCI-X.

Operational type is dependent on the operating mode of each bus. PCI-X uses block transfers based on ADQ and ADB concepts. While conventional PCI interfaces do not have the concept of ADQ and ADB, they observe the ADQ and ADB structures.

Each interface operates and places data into the queues and then dispatches the request to the other interface. A “valid” indication is used to determine when a request has been enqueued and is ready to be scheduled for being played out on the destination bus.

Other than for PCI Configuration space transactions the two buses are symmetrical. Each operates independently of the other bus, sending or receiving data from the queues.

3.10.1 PCI-to-PCI

PCI to PCI transactions use the ADQ Queue for all block transactions. Transactions can start and stop anywhere within an ADQ. Delayed transactions are supported using the same data and request queue structures that are used when operating in PCI-X mode. PCI to PCI-X.

3.10.2 PCI to PCI-X

When going from PCI to PCI-X, a given transaction can issue on the target bus after crossing at least one ADB, or upon transaction completion by the requestor on the initiating bus. Multiple ADB crossings would allow for larger transfers that have lower overhead on both buses.

Transactions originating from a conventional PCI initiator do not contain any of the PCI-X additional attributes such as byte count, and therefore the 31154 Bridge creates the attributes for the conventional PCI master before presenting the transaction onto the PCI-X bus. Write byte count, for example, is created based on what has been received by the bridge, and conversely, read byte counts are created based on prefetchable, and non prefetchable read policies described in Section 3.12.5.

3.10.3 PCI-X to PCI

Transactions to PCI can start as soon as the transaction is enqueued.

3.10.4 PCI-X to PCI-X

For the PCI-X to PCI-X case all transactions with the exception of immediate transactions play as unidirectional transactions. Each transaction plays until it is completed in one direction. No link is present to any transaction going in the opposite direction. Requests may result in multiple responses which each become an independent transaction.

3.11 Bus Interface Data Flow

Each bus interface of the bridge operates in one of four modes for a transaction in which it is involved. The following subsections describe the operation of each of the modes of operation.

- PCI as a target.
- PCI as a master.
- PCI-X as a target.
- PCI-X as a master.

3.11.1 Target Operation

The 31154 Bridge checks each operation to determine whether or not to assert DEVSEL# thereby claiming the transaction. The 31154 Bridge supports the standard set of bridge forwarding registers. When a transaction on the Origination Bus is within the standard set of defined forwarding ranges it is then forwarded to the Destination Bus.

Primary bus to Secondary bus “Base and Limit registers” define the ranges for transactions that are claimed and subsequently forwarded to the secondary bus interface. The 31154 Bridge , being a transparent bridge, utilizes inverse decoding for the purpose of claiming and forwarding transactions that are to be forwarded from the secondary bus to the primary bus.

3.11.1.1 As the PCI Target

As a PCI target, the 31154 Bridge enqueues requests and responds with a Retry while tracking a delayed transaction. After a request is enqueued it is ready to be forwarded to the Destination Bus (in accordance with ordering rules). A link between initial request and data operation is used to track data returning from Destination Bus.

Transactions start from the Origination Bus and issue on the Destination Bus. After a transaction is done on Destination Bus, operation completes when the initial master comes back one more time for the response.

The 31154 Bridge supports linear increment address mode only (AD[1:0]=00b), and disconnects conventional PCI memory transactions whose least significant two address bits are not 00b after a single DWORD.

For PMW operations, data is received before transaction is enqueued. At that point the byte count is known and the transaction can start on the Destination Bus. Using standard PCI protocol, 31154 Bridge will not insert wait states while receiving data but will disconnect a transaction whenever queue space is not available.

For delayed read operations, data received on the Destination Bus is held until the transaction is successfully completed by the Originating Bus Master. Data is sent to the Originating Master then using standard PCI protocol.

All prefetched read completion data is cleared from the internal queues if the corresponding transaction is disconnected by the Originating Master.

3.11.1.2 As the PCI-X Target

All transactions might have a Retry response if space is not available for either the data or the request itself. The 31154 Bridge receives data whenever it is the target of a Split Read Completion, PMW or, in the case of an immediate read data transfer on the bus, when the 31154 Bridge is the Master.

3.11.2 Master Operation

3.11.2.1 As the PCI Master

As PCI Master, the 31154 Bridge issues requests to a target, but does not insert wait states on PCI interface.

For PMW transactions, data is sent on Destination Bus until either byte count is satisfied, MLT expires, or Target disconnects.

For Prefetch operations, data is received until the transaction disconnects. Prefetch Disconnects from target are not retried. On Originating Bus, the 31154 Bridge returns only amount of data transferred before the Disconnect occurred. If the Originating Bus is operating in PCI-X mode, the 31154 Bridge fetches to the extent defined by the original requested byte count, and creates a single split completion sequence.

All other delayed transactions Retry until they complete, or a time-out error occurs. Status from the Destination bus operation is sent back to the Origination Bus.

Before a delayed transaction requests the bus, space must be available for a Split Completion entry going from the Destination to Origination Bus. If the transaction is a read, the 31154 Bridge checks for available space in the Destination to Origination data queue.

3.11.2.2 As the PCI-X Master

The 31154 Bridge tracks requests that is has issued as a PCI-X master until the full byte count of the transaction has been completed. This is done whether the operation has an immediate response or a Spit Response.

Transactions do not request the Destination Bus until a space is available in the D2O request queue. This space is required to accommodate an immediate response. Additionally, Block Read requests must have data space for at least two D2O ADQ blocks.

This operation might be repeated multiple times for a single Origination Bus request. Each time a disconnect occurs, or partial immediate response is received from Destination Bus target, address and byte count are updated. A new request is then generated based on the updated address and byte count.

This repeats until the full byte count has been transferred.

Transmittal of PMW data, Split Requests, and Split Completion data/status is performed by the master portion of the bus interface.

3.12 Conventional PCI Mode

The originating device for a given PCI bus segment broadcasts that the operating mode for the that bus is conventional PCI mode following reset if any device on the bus reports that it is incapable of running in PCI-X mode. The 31154 Bridge enters conventional PCI on the Primary Bus, whenever the bus mode is indicated to be conventional PCI by the upstream bridge. On the Secondary Bus 31154 Bridge enters conventional PCI mode following secondary reset when it has determined that at least one agent on the secondary bus reports that it is incapable of operating in PCI-X mode.

3.12.1 Posted Memory Write Transactions

The 31154 Bridge posts all Memory Write and Memory Write and Invalidate (MWI) transactions that are to be forwarded from one interface to the other. The 31154 Bridge accepts write data into its buffers without wait states. A posted memory write transaction is terminated when any of the following occur:

- the originator ends the transaction.
- insufficient buffer space exists to buffer another ADQ.

In the second case, target disconnect is returned to the originator.

The 31154 Bridge does not initiate a memory write transaction on the Destination bus until two ADQs of data have been captured during the transaction, or until the transaction is terminated by the originator. The 31154 Bridge does not insert master wait states when it acts as a bus master for the playing out of posted memory writes.

The 31154 Bridge ends the transaction when all of the posted data for this queue entry has been played out and accepted by the target on the Destination Bus.

The 31154 Bridge conditionally asserts P_SERR# if a target abort or master abort is detected on the target bus in response to the posted write.

3.12.2 Fast Back-to-Back Transactions

The 31154 Bridge accepts fast back-to-back transactions as a target, but will never generate them as an initiator.

3.12.3 Write Flow-Through

Write flow-through is supported opportunistically.

For example, a large burst write will be started on the target bus once two ADQs of data has been accumulated in the bridge. If the initiator continues the transaction for more than two ADQs then there will be simultaneous data transfers occurring on both the primary and secondary side.

3.12.4 Delayed Write Transactions

The 31154 Bridge executes delayed transactions when forwarding I/O and configuration writes from a conventional PCI interface to the other bus.

When an I/O or Configuration write transaction targeting the other PCI bus is first initiated, 31154 Bridge returns a target retry. The 31154 Bridge latches the transaction information, including address, bus command, write data, byte enables, REQ64# and PAR, and enqueues a delayed write request (DWR) if all of the following conditions are true at that time:

- space is available in the request queue structure.
- a transaction having the same address, bus command, write data, and byte enables does not already exist in the request queue structure.

The 31154 Bridge requests the destination bus and, once bus ownership is obtained, initiates the corresponding delayed write transaction in accordance with PCI ordering rules.

The 31154 Bridge always executes delayed write transactions as single data phase DWORD writes. Once the 31154 Bridge completes the destination bus delayed write transaction it adds the transaction completion status to origination side request queue status structure. Completion status returns termination mode (TRDY#, target abort, master abort) and whether PERR# assertion was detected during delayed write transaction. This phase of delayed transaction is called delayed write completion (DWC).

When originator repeats transaction using same transaction information, the 31154 Bridge either retries the originator indicating that the delayed write transaction has not yet completed, or target disconnects the transaction with either TRDY# (normal completion) or Target Abort (error indication).

3.12.4.1 Delayed Write Transaction Time-out Errors on the Origination Bus

When the 31154 Bridge has delayed write transaction completion status for an originator and the originator does not repeat the initial transaction before the Discard Timer for that interface expires, (see Bridge Control Register Offset 3Eh, and 31154 Bridge Control 1 Register Offset 6Ch), the 31154 Bridge discards the delayed transaction freeing up both request and completion queue space for re-allocation to a future delayed transaction. If configured to do so via the Discard Timer SERR# Enable bit of the Bridge Control Register, 31154 Bridge also asserts SERR# on its primary bus in the event that the delayed transaction had timed out and had been discarded by the 31154 Bridge .

The timer starts when Completion Status is available. The Discard Timer is reset when the transaction which started the timer completes.

3.12.5 Read Transactions

3.12.5.1 Delayed Read Transactions

Delayed read transaction protocol is similar to that of delayed write transactions, with the exception that transfers longer than a DWORD may also utilize delayed read transactions, specifically delayed memory read transactions. When a read to I/O, configuration, or memory intended for the other PCI bus is first initiated, the 31154 Bridge returns a target retry. The 31154 Bridge enqueues the transaction information, including address, bus command, byte enables for non-prefetchable reads, and REQ64# if all of the following conditions are true:

- space is available in the request queue structure.
- a delayed request having the same address, bus width, and bus command does not already exist in the request queue structure.

This phase of the delayed transaction is called a delayed read request (DRR).

The 31154 Bridge then requests the destination bus and, once it obtains bus ownership, initiates the delayed read request (read transaction) in accordance with PCI ordering rules. If the transaction is a non-prefetchable read, then 31154 Bridge requests only a single DWORD of data. If the transaction is a memory read to a pre-fetchable memory space, then the 31154 Bridge will pre-fetch a programmable amount of data. Refer to Section 3.12.5.4, “Prefetching” on page 61 for details.

The 31154 Bridge completes the transaction on the destination bus[1], and stores response to the appropriate queues. This phase of the delayed transaction is called the delayed read completion (DRC).

When a read transaction on the Origination Bus matches a delayed read transaction having a DRC, the 31154 Bridge returns the read data, data parity bit(s), and appropriate target termination in accordance with PCI ordering rules. For all memory read transactions, the 31154 Bridge aliases the memory read, memory read line, and memory read multiple commands when comparing a transaction in the delayed transaction queue to one initiated on the Origination PCI bus. Therefore, regardless of exact command used, if the address matches, and both commands are any type of memory read, the 31154 Bridge considers it a match. If there is no match or, the ordering rules prevent returning the completion data at that point, the 31154 Bridge returns target retry. The target terminations returned are as follows:

Table 26. Target Termination Returns

Destination Bus Target Response to Intel® 31154 Bridge	Intel® 31154 Bridge response to Originator
TRDY#	TRDY# (with STOP# when returning last data phase)
Target Abort	Target Abort
Master Abort	• TRDY# and FFFFFFFFh (if Master Abort Mode bit = 0)· • Target Abort (if Master Abort Mode bit = 1)

1. Which might execute as another delayed read transaction, for example if the target is another bridge device also executing a delayed read transaction.

3.12.5.1.1 Delayed Read Transaction Time-out Errors on Origination Bus

When the 31154 Bridge has read completion data for an originator and the originator does not repeat the initial transaction before the Discard Timer for that interface expires (if enabled), (see Bridge Control Register Offset 3Eh, and 31154 Bridge Control 1 Register Offset 44h), the 31154 Bridge discards the delayed transaction. If configured to do so via the Discard Timer SERR# Enable bit of the Bridge Control Register (offset 3Eh), the 31154 Bridge will also assert SERR# on its primary bus in the event that the delayed transaction had timed out and been discarded.

3.12.5.2 Non-prefetchable Reads

The following transactions are considered by the 31154 Bridge to be non-prefetchable:

- I/O transactions.
- configuration transactions.
- transactions using the Memory Read, Memory Read Line, or Memory Read Multiple commands that address the non-prefetchable memory range.
- Single DWORD Memory Read, Memory Read Line, or Memory Read Multiple transactions.

When originating a non-prefetchable read, the 31154 Bridge requests only a single DWORD of read data from the target. The 31154 Bridge uses the same byte enables driven by the originator of the transaction[1].

When the 31154 Bridge returns the read data to the originator, it asserts STOP# with TRDY# to enforce a single DWORD transaction.

1. This is the case where FRAME# is de-asserted for the first data phase, and REQ64# was never asserted.

3.12.5.3 Read Flow Through

Read Flow Through can be either fine grained or large grained. For the fine grained case data is tracked on each cache line boundary using an additional tracking mechanism. Large grained tracking is done at the ADB level passing data between the interfaces when a full ADQ is available for the transaction.

Flow-through is achieved when data is transferring on both the Origination Bus and Destination Bus at the same time. The 31154 Bridge stops issuing Retry when a valid DRC from the Destination Bus is indicated to the Origination Bus.

3.12.5.3.1 Fine Grained Tracking

Fine grained tracking provides the greatest flexibility. Fine grain data tracking occurs at the cache line level allowing each interface to use either a 32- or 64-bit width for a transfer.

Using a fine grain tracking mechanism is particularly useful for PCI-to-PCI tracking, allowing each data transfer to proceed across the bridge as soon as it becomes available and allowing wait state insertion on a data phase basis. Fine grain tracking is employed whenever forwarding data to a bus of less than or equal bandwidth.

The insertion of wait states on each data phase is attractive because of the eight clock rule on PCI for consecutive data phases. Large grain tracking has the sum of the delays of all the data phases in an ADQ. Large grain tracking must wait longer to start transferring, and is more likely to disconnect due to eight or more clocks of accumulated delay.

3.12.5.3.2 Large Grained Tracking

Large grained tracking is done at the ADQ level. Each time a transfer on the Destination Bus crosses an ADB, that ADQ may be transferred onto the Origination Bus. This is the policy that is executed whenever the transaction is a PMW or the Originating Bus is operating in PCI-X mode.

3.12.5.4 Prefetching

The 31154 Bridge supports a staged pre-fetch mechanism that enables fine tuning of how much data to pre-fetch. The feature remembers, from past experience, whether or not the needs of the initiator were sufficiently met, or whether even more data should be pre-fetched for a given transaction.

Prefetching is performed for memory read transactions when targeting prefetchable memory. The amount of data prefetched by the 31154 Bridge is programmable. If the prefetch size from one of the following tables is greater than 128 bytes, the 31154 Bridge disconnects at the last ADB it crosses.

Prefetch management uses a multiplication factor to determine the amount of data to be prefetched. Two sets of Prefetch factors are used, one for the Primary Bus and another for the Secondary Bus. The Secondary Bus has four control bits that select when a prefetch factor is applied to operations based on the REQ/GNT pairs. The first three REQ/GNT[2:0] pairs have individual enables for the prefetch factor, while the remaining REQ/GNT pairs [8:3] are controlled by a single control bit.

Disabling the prefetch factor results in the use of a prefetch factor equal to zero during all prefetch operations.

Note: If the 31154 Bridge internal arbiter is disabled, all secondary bus agents are enabled to use the FirstRead/ReRead secondary bus factor values, ignoring the REQ#GNT# enable bits.

The 31154 Bridge uses the 64-bit extension signals to initiate and complete prefetchable read transactions as a master. As a target 31154 Bridge asserts ACK64# in response to an originator's assertion of REQ64# for read transactions to prefetchable memory[1].

Prefetch factors are divided into two types, FirstRead and ReRead Factors. These factors are stored in the PF_POLICY register; (see Section 5.2.8, “Offset 50H: MTT - Multi-Transaction Timer” on page 115), and are used to compute the amount of data prefetched as shown in Table 27. The “(Factor+1)” value of the same table adds 1 to either the FirstRead or ReRead factors, depending upon whether the request is the first, or a continuing sequence.

The 31154 Bridge determines whether a transaction might continue by looking for the following combination of events when the Master completes a prefetched transaction on the Origination Bus.

- The 31154 Bridge disconnects the transaction because data is exhausted.
- The Master still has FRAME# asserted at the disconnect.

This results in the 31154 Bridge storing the beginning address of cacheline. Up to eight beginning addresses are stored by the 31154 Bridge for prefetch ReRead transactions.

Every MR, MRL, and MRM transaction is compared to these stored values. When a match is detected the byte count is set based on the ReRead value. When a match does not occur the FirstRead value determines the byte count.

Prefetchable amounts are not guaranteed; if the queue fills before the full amount is prefetched then the 31154 Bridge disconnects the target and only returns the amount of data buffered.

1. Refer to Section 3.6, “64-Bit Operation” on page 44.

Table 27. Prefetch Data Length

Memory Operation	Alignment	Read Size
Read	4 * DWORD	(Factor +1) * 4 * DWORD
Read Line	cacheline	(Factor +1) * cacheline
Read Multiple	2 cachelines	(Factor +1) *2* cachelines

Prefetch size, in bytes, for Read, ReadLine Read Multiple transactions are shown in Table 28 through, Table 30 respectively[1].

Table 28. Read Command Prefetch Size

Factor	Bytes
0	16
1	32
2	48
3	64
4	80
5	96
6	112
7	128

Table 29. Read Line Command Prefetch Size

Factor	Cache Line Size	
	32	64
0	32	64
1	64	128
2	96	192
3	128	256
4	160	320
5	192	384
6	224	448
7	256	512

Table 30. Read Multiple Prefetch Size

Factor	Cache Line Size	
	32	64
0	64	128
1	128	256
2	192	384
3	256	512
4	320	640
5	384	768
6	448	896
7	512	1024

1. The cache line size is a power of two. Masters should only start on a cache line boundary.

3.12.5.4.1 FirstRead

The FirstRead value determines how much data is read on the FirstRead transaction for a given originator. Each type of read command (e.g., MEM_Rd MRM, MRL) prefetches the amount of data specified in Table 28 through Table 30.

Requests not stating on cache line boundary are aligned to cache line at end of FirstRead transaction.

3.12.5.4.2 ReRead (repeated until time-out)

The ReRead value determines how much data is read on the ReRead transaction for a given originator. Each type of read command (e.g., MEM_Rd MRM, MRL) prefetches the amount of data specified in Table 28 through Table 30.

3.12.6 Transaction Ordering

Transaction ordering for all data traveling in the same direction across the bridge adheres to the conventional PCI set of ordering rules. Note that all “Don't Care” (i.e., yes/no) entries are implemented as “yes” providing the maximum opportunity for making forward progress. There are no ordering requirements for transactions traveling in opposite directions.

Table 31. Conventional PCI Ordering Rules

Row Pass Column?	PMW (Column 2)	DRR (Column 3)	DWR (Column 4)	DRC (Column 5)	DWC (Column 6)
PMW (Row 1)	No	Yes	Yes	Yes	Yes
DRR (Row 2)	No	Yes	Yes	Yes	Yes
DWR (Row 3)	No	Yes	Yes	Yes	Yes
DCR (Row 4)	No	Yes	Yes	Yes	Yes
DWC (Row 5)	Yes	Yes	Yes	Yes	Yes

3.13 PCI-X Bus Mode

The 31154 Bridge behavior when dealing with areas of PCI-X operation that are open to interpretation is highlighted. Please see the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a for all details related to PCI-X operation.

Unless otherwise noted in this section, the 31154 Bridge follows all rules of the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.

3.13.1 Attributes

Table 32 describes how 31154 Bridge handles a few of the less well defined attribute fields.

Table 32. 31154 Bridge Implementation of Requester Attribute Fields

Attribute	Function
No Snoop (NS)	As a target, this bit is forwarded with the transaction to allow a north bridge to not snoop the transaction. The 31154 Bridge takes no action on this bit.
Relaxed Ordering (RO)	This bit allows relaxed ordering of transactions, which the 31154 Bridge does not permit. This bit is simply forwarded by 31154 Bridge, and is never initially set by the 31154 Bridge.
Tag	The 31154 Bridge stores and forwards tag information presented to it by the original requester. The only exception to this behavior is when the 31154 Bridge must forward a request on behalf of a conventional PCI requester. In this case there isn't any tag (or other Sequence ID attributes) available, and the 31154 Bridge creates one for the sequence.

3.13.2 Special Notes for Burst Transactions

The *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a allows burst transactions to cross the minimum memory map boundary (in the 31154 Bridge case, this is 1 M) and 4 GB address boundaries. The 31154 Bridge will never do this as an originator or as a target. It will always end the transaction at a 1M boundary with an exception for Block Read Transactions which are handled as per the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a. As a target, it disconnects transactions on these boundaries.

The 31154 Bridge will never issue an immediate response as a target for a burst read command, but it must be ready with 256 bytes of data space (two ADQs) when originating one. If it does not have this space available, it will not issue the transaction and wait for the internal congestion to resolve naturally.

3.13.3 Split Transactions

3.13.3.1 Completer Attributes

Completer attributes are normally passed through the 31154 Bridge without modification. However, certain error or other conditions may cause the 31154 Bridge to modify these bits.

Additionally, whenever an immediate response is received the 31154 Bridge becomes the completer and must report any error conditions it encounters in handling the transaction.

Table 33. 31154 Bridge Implementation Completer Attribute Fields

Attribute	Function
Byte Count Modified (BCM)	This bit is used for diagnostic purposes. The 31154 Bridge forwards this bit, but might also generates it as specified by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.
Split Completion Error (SCE)	31154 Bridge sets this bit in accordance with the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a (or later) specification
Split Completion Message (SCM)	31154 Bridge returns an SCM in the event that an error, corresponding to the current sequence has been detected. 31154 Bridge also returns an SCM whenever completing a split write transaction.

3.13.3.2 Requirements for Accepting Split Completions

The 31154 Bridge will claim Split Completions targeting resources on its other side provided the following conditions are met:

- At least two ADQ of buffer space is available (otherwise the Split Completion will be retried).
- The Sequence ID matches an outstanding Split Request that had been issued by 31154 Bridge.
- There are less than two Split Completion of the same sequence ID currently staged within the 31154 Bridge internal buffers[1].

3.13.3.3 Split Completion Messages

Split Completion messages provide a means of reporting, to the requestor, status information relating to the current completion transaction. An SCM received by the 31154 Bridge is passed to the other bus unaltered.

The 31154 Bridge generates a Split Completion Message (SCM) when it has encountered an error with a transaction on the Destination Bus. SCMs are issued for error conditions including Master, or Target Abort encountered on the Destination Bus, as well as for error conditions relating to corrupted completion transactions. In such cases the 31154 Bridge will forward an SCM reporting the error condition to the original requestor.

Additionally the 31154 Bridge generates an SCM for split write transactions that are completed on the destination bus as an immediate transaction.

Refer to Section 6, “Error Detection and Reporting” on page 157 for a complete, detailed description of error handling.

1. 31154 Bridge allows up to two SCs of the same sequence ID on the bridge at any given time. If a third Split Completion of the same sequence ID targets 31154 Bridge, it will be Retried.

3.13.4 Transaction Ordering

Transaction ordering for all data traveling in the same direction across the bridge adheres to the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a ordering rules for bridges. Note that all "Don't Care" choices (i.e., yes/no entries) have been chosen to align completely with the ordering policy for conventional PCI Mode. By making the same policy decisions regarding the ordering of transactions flowing out of the bridge, the logic for controlling transaction queuing is greatly simplified. There are no ordering requirements for transactions traveling in opposite directions.

Table 34. PCI-X Ordering Rules

Row Pass Column?	Memory Write (Column 2)	Split Read Request (Column 3)	Split Write Request (Column 4)	Split Read (Column 5)	Split Write (Column 6)
Memory Write (Row A)	No[a]	Yes	Yes	Yes	Yes
Split Read Request (Row B)	No	Yes	Yes	Yes	Yes
Split Write Request (Row C)	No	Yes	Yes	Yes	Yes
Split Read (Row D)	No[b]	Yes	Yes	Yes[c]	Yes
Split Write (Row E)	Yes	Yes	Yes	Yes	Yes

a. 31154 Bridge ignores the Relaxed Ordering bit, and so therefore will not allow a PMW to pass a previously posted PMW.
b. 31154 Bridge ignores the Relaxed Ordering bit, and so therefore will not allow a Split Read Completion to pass a previously posted PMW.
c. 31154 Bridge will allow Split Completions possessing different Sequence IDs to pass each. Split Completions possessing the same Sequence ID must play out in the order that they were received. 31154 Bridge will accept two such Split Completions on chip at any given time.

3.13.5 Transaction Termination as a PCI-X Target

3.13.5.1 Retry

The 31154 Bridge will retry a transaction when any of the following conditions is true:

- Target queue (Request queue) is full.
- When a Serial ROM pre-load is in progress.
- When receiving a third Split Completion of the same sequence (31154 Bridge allows a maximum of two on chip at any time).

The 31154 Bridge stores no state from a transaction that it has target terminated with retry.

Retries due to buffer full conditions should be infrequent as the 31154 Bridge supports a deep request queue for pending operations. Additionally, a Split Queue keeps transactions that are in process, between a Split Response and the final Split Completion for that sequence.

Note: To support the "device hiding" features of a Compact PCI Hot Swap system, the 31154 Bridge will not claim transactions while the Serial ROM pre-load is in progress if the HS_SM strap is asserted. This will result in a Master Abort condition on the primary bus.

3.13.5.2 Split Response

The 31154 Bridge responds to all "splitable" transactions[1] with a Split Response, if not retried due to insufficient buffer availability. One exception to this is for PCI Configuration read cycles targeting the 31154 Bridge internal configuration registers.

3.13.5.3 Split Completion Errors

During the address phase the 31154 Bridge looks for an exact Sequence ID match between a split completion transaction on the bus with any pending completion enqueued within its corresponding Split Queue. Unless there is an exact match, a split completion transaction that would appear to be targeting an agent on the opposite side of the bridge is ignored, causing the Completer to Master Abort.

The bridge will generate a target abort if the Sequence ID matches but a byte count error is detected within the completion attribute phase.

Refer to Section 6, "Error Detection and Reporting" on page 157 for additional details.

3.13.6 Bridge Buffer Requirements

The 31154 Bridge always has at least 256 bytes (2 ADQ) in use by a PMW or reserved for incoming PMW transactions. The 31154 Bridge does not implement the split completion buffer pre-allocation algorithm as proposed by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.

1. All transactions except for Split Completion, Memory Write, and Memory Write Block transactions which are immediate transactions, and so cannot be converted to split transactions.

3.14 Compact PCI

3.14.1 Compact PCI Hot Swap

The 31154 Bridge meets the standard requirements to be considered “Hot Swap Silicon”.

Hot Swap Control and Status Register is implemented via the Extended Capability Pointer mechanism in the Function 0 configuration space (Section 5.3.4, “CompactPCI* Hot Swap” on page 147).

Provides Software Connection Control Resources for ENUM#, Hot Swap Switch, blue LED and Device Hiding.

Handle Switch de-bouncing is implemented.

The bridge is Initially Not Responding on its primary interface when configured for Hot Swap Mode Select.

See Section 3.4.1.3, “Compact PCI Hot Swap Mode Select” for a description of HS_SM and HS_FREQ[1:0] requirements.

3.14.2 Support for Dual-Host cPCI Configurations

In addition to the compact PCI Hot Swap model, the 31154 Bridge has hardware support for Dual-Host cPCI Configurations. Through the use of NT_MASK, S_ARB_LOCK and S_TRISTATE the system can flush the data queues, quiesce the bus, and isolate the bridge to allow another bridge to assume central resource functionality.

In order to isolate the bridge from the secondary bus, the bus master enable bit (Section 5.1.2, “Offset 04H: CMD - Command” on page 80) must be programmed to ‘0’ (default value). This will prevent the bridge from claiming transactions on the secondary interface.

One possible method for transferring control from one bridge to another is detailed below:

Original host bridge will flush its queues via the NT_MASK/QE handshake defined in Section 3.8, “Flush Buffers Feature”. Following the buffer flush, the S_ARB_LOCK pin can be asserted to quiesce the bus by locking the arbiter to the bridge. At this point the S_TRISTATE pin on the original host bridge can be asserted and the stand-by bridge can have its S_TRISTATE pin deassert to allow it to generate clocks and GNT# outputs. The new bridge can now program its configuration space, enable bus mastering and assume control of the secondary bus.

To prevent Grant Time-out scenarios from blocking a requesting agent the stand-by bridge should pre-load the Section 5.2.3, “Offset 44H: VCR1 - 31154 Bridge Control Register 1” on page 108 to disable the GRANT# time-out by programming bit 04 to ‘1’.

Note: System behavior is indeterminate if S_TRISTATE transitions while there is activity on the secondary bus.

Arbitration 4

The 31154 133MHz PCI Bridge provides an integrated secondary bus arbiter. The internal arbiter is enabled if, at the low-to-high trailing edge of P_RST# the ARB_DISABLE pin strap is sampled at a logic low level.

Optimum bridge performance is typically achieved when operating with the integrated secondary bus arbiter enabled. The internal arbiter is able to make more intelligent arbitration decisions based on information available to it internally; information not typically available external to the bridge.

4.1 Arbitration Events

An arbitration event is defined as the act of evaluating all bus requests, applying arbitration policy algorithms, and assigning a new bus grant. Within a busy environment PCI arbitration events occur in a “hidden” fashion, where the next bus owner is chosen during the current bus transaction thereby minimizing bus latency in turning the bus over to its new owner.

Aside from performing arbitration events within an active environment, two other cases exist:

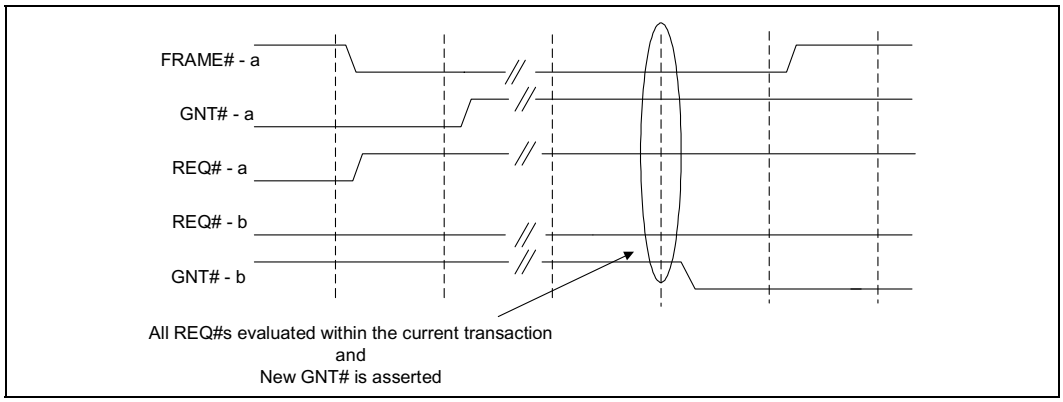
- Idle bus with no pending requests (bus parking).
- Granted agent is non-responsive (Grant Time-out situation).

4.1.1 Arbitrating in Traffic

The 31154 133MHz PCI Bridge secondary bus arbiter always performs arbitration events for an active secondary bus during execution of the current transaction, effectively “hiding” any additional latencies when turning the bus over to it's next owner. Independent of the secondary bus mode of operation (conventional PCI or PCI-X), the 31154 133MHz PCI Bridge always performs an arbitration event as follows:

1. De-assert the current GNT# as soon as 31154 133MHz PCI Bridge has observed that the new bus owner has begun the next bus transaction (i.e., FRAME# assertion sampled).
2. Within the current transaction, the 31154 133MHz PCI Bridge evaluates all outstanding bus requests and determines which agent will be granted the bus next.
3. GNT# is asserted to the next bus owner while the current transaction is executing.

Figure 6. Arbitration Events



4.1.2 Bus Parking

When the secondary bus is idle with no pending bus requests, the 31154 133MHz PCI Bridge arbiter will park bus ownership with either the last granted agent or itself depending on the programming of the Secondary Bus Arbiter Control register.

When emerging from S_RST# the secondary bus is always internally parked at the 31154 133MHz PCI Bridge if its secondary arbiter is enabled.

Refer to Section 5.2.1, “Offset 41H: ARB_CSR - Secondary Arbiter Control /Status Register” on page 104 for details on the ARB_CSR device specific register (offset 41h).

4.1.3 Arbiter Lock

When the ARB_DISABLE pin is sampled high at anytime after reset, the arbiter (if enabled) will go into a lock state and only give grant to the 31154 133MHz PCI Bridge. The bridge will allow the current transaction to complete and then it will only grant the bus to itself.

4.1.4 Grant Time-Out

Once a grant has been asserted on the bus, and the bus has gone idle, the granted agent is required to begin its initial transaction, indicated by the assertion of FRAME# within a maximum number of clocks. When the 31154 133MHz PCI Bridge secondary bus is operating in conventional PCI mode, the maximum permissible delay is 16 clocks. When the 31154 133MHz PCI Bridge secondary bus is operating in PCI-X mode, the maximum permissible delay is 6 clocks. This requirement intends to ensure that PCI agents do not request the bus unless they are prepared to use it. This mechanism can be disabled via GRANT Time-out Disable bit of VCR1 register (offset 44h).

The 31154 133MHz PCI Bridge employs a Grant Time-out counter mechanism that begins counting from the time the bus goes to the idle state with a bus grant asserted. If FRAME# is not sampled in the asserted state by the granted agent before the time-out counter expires, the agent's grant is de-asserted, and a new arbitration event occurs. Note that in an idle, bus parked situation, the Grant Time-out counter does not apply.

Agents that are slow to assert FRAME# may, when operating on a busy bus, be starved as a result of their PCI non-compliant behavior.

For diagnostic purposes, status information detailing the detection of a Grant Time-out along with information as to which secondary agent was in violation of the specification, is available in the ARB_CSR register.

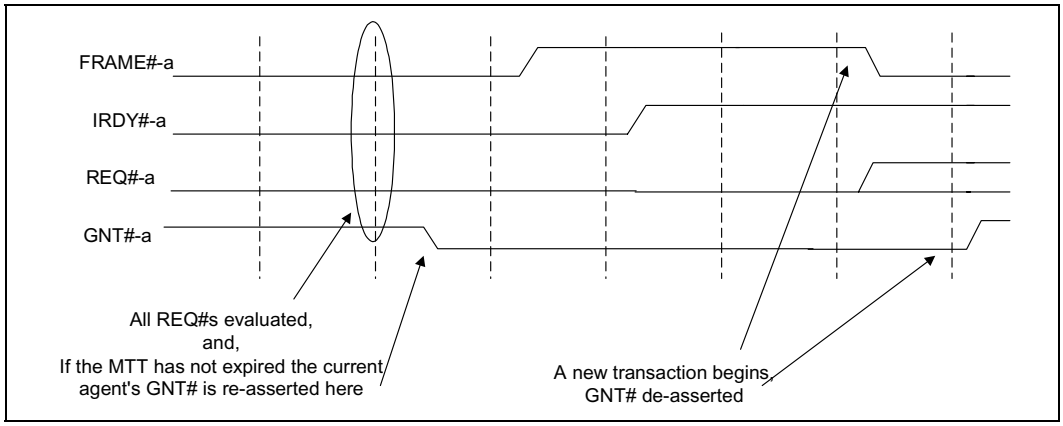
Refer to Section 5.2.1, “Offset 41H: ARB_CSR - Secondary Arbiter Control /Status Register” on page 104 for details on the ARB_CSR device specific register (offset 41h).

4.2 Multi-Transaction Timer (MTT)

The 31154 133MHz PCI Bridge incorporates a multi-transaction timer that, in conjunction with the granted agent MLT and the Grant Time-out mechanism, enables the grantee to perform multiple transactions within a single arbitration cycle. Whereas an agent MLT governs the maximum duration of a single PCI transaction, the MTT residing in the secondary arbiter block, enables multiple PCI transactions to proceed by effectively establishing a minimum grant time period.

One MTT counter/value supports all secondary bus agents. Mask bits individually enable, or disable the MTT for each agent on the secondary bus.

Figure 7. Multi-Transaction Timer Operation



For MTT programming model details refer to Section 5.2.8, “Offset 50H: MTT - Multi-Transaction Timer” on page 115.

4.2.1 MTT Rules

- The MTT counter is loaded with its programmed value each time, as a result of an arbitration event, a GNT# is asserted to an agent other than the last bus owner with an exception case for a bus parked situation. When the bus is in an idle, parked GNT# situation the MTT programmed value will be re-loaded each time the park agent's GNT# is re-asserted.
- The MTT countdown begins when the granted agent's initial assertion of FRAME# is sampled by the 31154 133MHz PCI Bridge on the bus.
- An agent wishing to utilize the MTT is required to continually assert its REQ# signal throughout the current transaction in it's entirety. If at any time during the current transaction the agent de-asserts the REQ# signal, MTT usage is terminated for the remainder of the current arbitration cycle.
- No greater than four transactions will be re-granted by the 31154 133MHz PCI Bridge during any single arbitration cycle, regardless of whether or not the MTT had expired.

If the following three conditions are satisfied at the next arbitration event, the 31154 133MHz PCI Bridge arbiter re-asserts the current owner's GNT# enabling a new transaction to begin from the same secondary bus agent.

- The current bus owner REQ# is sampled asserted, having never been de-asserted throughout the current transaction.
- The MTT count has not yet expired.
- The number of consecutive transactions already executed by this same bus agent is three or less.

For each subsequent transaction within the same arbitration cycle the grantee MLT is re-initialized to its programmed value, while the MTT continues to count down. If during a transaction the grantee's MLT expires, the grantee should self evict, and de-assert its REQ# thereby ending its current ownership of the bus.

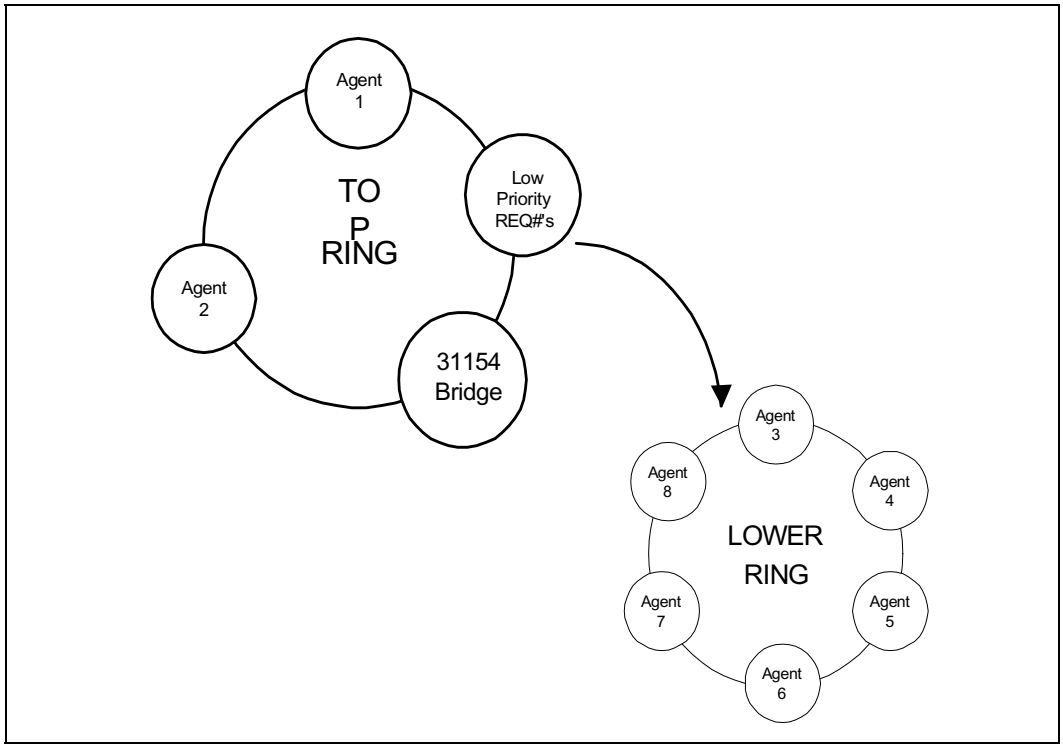
4.3 Conventional PCI Arbitration

When operating in conventional PCI mode, the 31154 133MHz PCI Bridge conducts arbitration using a two tiered “round robin” rotating scheme (Figure 8).

When the 31154 133MHz PCI Bridge owns the bus it plays out any newly enqueued delayed transaction requests, or PMW data in accordance with PCI ordering rules.

Bus agents can be programmed to reside in the high (top), or lower priority ring of arbitration. Refer to Section 5.2.1, “Offset 41H: ARB_CSR - Secondary Arbiter Control /Status Register” on page 104 for detailed programming interface information.

Figure 8. Two-Tiered Round Robin Rotating Scheme



4.4 PCI-X Arbitration

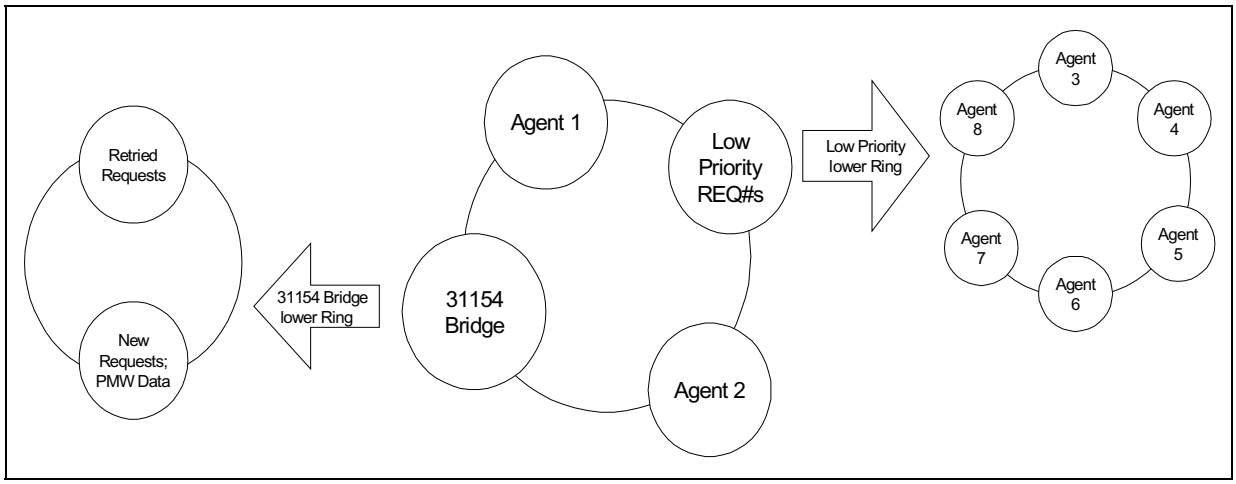
The 31154 133MHz PCI Bridge secondary arbitration scheme for PCI-X mode is nearly identical to that of its conventional PCI arbitration scheme. The only real difference is that when the secondary bus is running in PCI-X mode, the 31154 133MHz PCI Bridge requests the bus for playing out split completions, as well as for playing out new split requests and PMW immediate data.

4.4.1 Fair Internal Arbitration

Split Completions, new internal requests, and posted Memory Write data are rotated fairly when determining the next transaction to be played out of the 31154 133MHz PCI Bridge on its next bus ownership. Due to the effect of the MLT, the 31154 133MHz PCI Bridge interleaves other valid split completions in an attempt to promote more uniform forward progress for all agents through the bridge.

Figure 9 below illustrates the PCI-X arbitration scheme.

Figure 9. PCI-X Priority Rings



4.4.2 Retry or Disconnected Request

When a 31154 133MHz PCI Bridge mastered transaction receives either a Target Retry or other Target Disconnect response, the 31154 133MHz PCI Bridge internal transaction flow arbiter[1] ensures that this particular internal request is masked until all other currently outstanding requests have been honored. In a sense this could be viewed as a third level lower arbitration ring for the 31154 133MHz PCI Bridge that is underneath the “New Internal Requests” ring.

Request masking is only done for internal requests that have been target terminated. The 31154 133MHz PCI Bridge does not block grants to external agents based on Retry or a Disconnect. External agents may have multiple functions with request streams active that are not related to the request that was retried. External agents simply wait for their next slot in the normal arbitration queue.

1. Arbiter/control logic that determines which of the valid internal transactions plays out next. Not to be confused with the PCI bus arbiter.

Programming Interface 5

The 31154 Bridge programming interface is provided in the configuration register address space, and is accessible only from the primary bus interface. The space is divided into four groups with the ranges indicated in Table 35.

Table 35. Configuration Register Address Space Groupings and Ranges

Register Group	Configuration Offset
Standard PCI Configuration	00-3Fh
Device Specific Registers	40-77h
Reserved	78-D3h
Enhanced Capability List	D4-FFh

Details of three of these four groups are given in the following subsections. The Reserved section needs no further explanation.

The following sections define the 31154 Bridge programming interface. In addition to the minimum standard set of PCI-to-PCI bridge features, the 31154 Bridge also supports several device specific features as well as other PCI standard enhanced capabilities. The PCI enhanced capabilities supported are shown in Table 36.

Table 36. PCI Enhanced Capabilities Supported

Enhanced Capability	Configuration Offset
Chassis/Slot Identification	D4h
PCI Bus Power Management (PCI-PM) Revision 1.1	DCh
VPD (Vital Product Data)	E4h
Compact PCI Hot Swap Revision 2.1 R2.0	ECh
PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a	F0h

PCI enhanced capabilities are enumerated, and managed via the PCI standard Capabilities linked list infrastructure. System software discovers the existence of enhanced capabilities by sampling the state of the PCI Status Register (Offset 06h). Bit(4) of the PCI Status Register sampled as a 1b indicates that a capabilities linked list for at least one enhanced capability exits, beginning at the address offset contained in the Capabilities Pointer register, located at offset 34h.

Table 35 through Table 37 provide an overview of the 31154 Bridge Configuration Space Registers. Detailed register definitions follow each table.

Note: Some register bits have defined behavior that differs depending upon the mode of the subject interface. (i.e., Conventional PCI or PCI-X). In such cases the behavior is explicitly spelled out for each mode. In all other cases the stated definition applies to both modes of operation.

5.1 Standard PCI Configuration Header Registers (Offset 00H-3FH)

Table 37. Standard PCI Type 1 Configuration Space Address Map

Byte 3	Byte 2	Byte 1	Byte 0	Byte Offset
Device ID$^{\Psi}$		Vendor ID$^{\Psi}$		00h
Primary Status		Primary Command		04h
Class Code			RevID$^{\Psi}$	08h
(reserved)	Header Type	Primary MLT	Primary CLS	0Ch
Reserved				10h
Reserved				14h
Secondary MLT	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		IO Limit	IO Base	1Ch
Non-prefetchable Memory Limit Address		Non-prefetchable Memory Base Address		20h
Prefetchable Memory Limit Address		Prefetchable Memory Base Address		24h
Prefetchable Memory Base Address Upper 32 Bits				28h
Prefetchable Memory Limit Address Upper 32 Bits				2Ch
IO Limit Upper 16 Bits		IO Base Upper 16		30h
Reserved			Capabilities Pointer	34h
Reserved				38h
Bridge Control		Primary Interrupt Pin	Reserved	3Ch

Note: Registers named in Table 37 that are suffixed with a ψ symbol, may be pre-loaded using the serial ROM interface.

The following subsections detail the bit assignments, and corresponding definitions for each of the the 31154 Bridge standard PCI configuration Type 1 header registers.

Register bits of the type “RC” (Read Clear) are readable, and writeable only to the extent that they are cleared by writing a 1b to them. Writing 0b to a RC bit has no affect on the current state of the bit.

Register bits of the type “Reserved” return 0b when read, and writes to them have no affect.

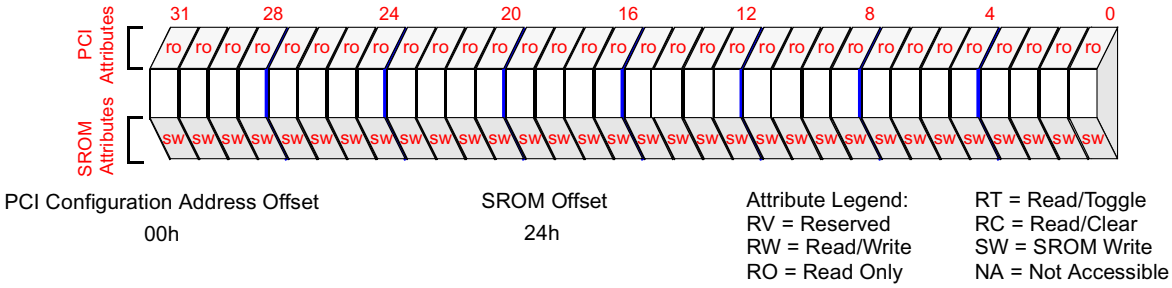
Default power on reset states are provided for all but those fields that are device dependent. Device specific defaults are labeled “-”.

5.1.1 Offset 00H: ID - Identifiers

Contains the vendor and device identifiers.

This register is pre-loadable by setting offset 00h of the Serial ROM to 1000_0001b.

Table 38. ID - Identifiers



PCI Configuration Address Offset
00h

SROM Offset
24h

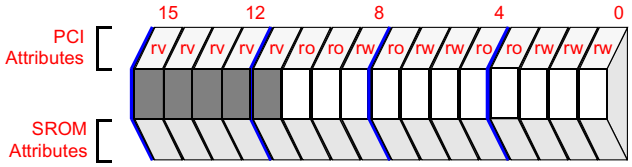
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:16	537C	Device ID (DID): Indicates the unique device ID that is assigned to the 31154 Bridge by the PCI SIG.
15:00	8086h	Vendor ID (VID): 16-bit field which indicates that Intel is the vendor.

5.1.2 Offset 04H: CMD - Command

Controls how the 31154 Bridge behaves on its primary interface, and is the same as all other devices, with the exception of the VGA Palette Snoop bit. As this component is a bridge, additional command information is located in a separate register called “Bridge Control” located at offset 3Eh.

Table 39. CMD - Command (Sheet 1 of 2)



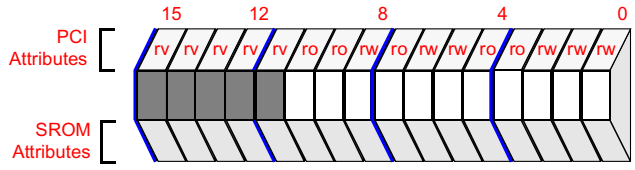
PCI Configuration Address Offset
04h

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:11	00h	Reserved
10	0b	Interrupt Disable This bit disables the bridge from asserting INTx#. This bit is read only and has no affect on bridge operation.
09	0b	FB2B Enable: Enables/Disables the generation of fast back to back transactions on the primary bus. the 31154 Bridge does not generate fast back to back transactions on the primary bus.
08	0b	SERR# Enable (SEE): Enables primary bus SERR# assertions. 0b = the 31154 Bridge will not assert P_SERR#. 1b = the 31154 Bridge may assert P_SERR#, subject to other programmable criteria.
07	0b	Wait Cycle Control (WCC): Always returns 0b indicating that the 31154 Bridge does not perform address or data stepping,
06	0b	Parity Error Response (PER): Controls the 31154 Bridge response to a detected primary bus parity error. 0b = If a data parity error is detected the 31154 Bridge does not assert P_PERR#. Also the 31154 Bridge does not assert P_SERR# in response to a detected address or attribute parity error. 1b = If a data parity error is detected the 31154 Bridge asserts P_PERR#. the 31154 Bridge also asserts P_SERR# (if enabled globally via bit(8) of this register) in response to a detected address or attribute parity error.
05	0b	VGA Palette Snoop Enable (VGA_PSE): Controls the 31154 Bridge response to VGA-compatible palette write transactions. VGA palette write transactions are I/O transactions whose address bits are: • P_AD[9:0] equal to 3C6h, 3C8h or 3C9h. • P_AD[15:10] are not decoded (i.e. aliases are claimed), or are fully decoding (i.e., must be all 0's depending upon the VGA aliasing bit in the Bridge Control Register, offset 3Eh. • P_AD[31:16] equal to 0000h. 0b = the 31154 Bridge ignores VGA palette write transactions, unless decoded by the standard I/O address range window. 1b = the 31154 Bridge responds to VGA palette write transactions with medium DEVSEL# timing and forwards them to the secondary bus.

Table 39. CMD - Command (Sheet 2 of 2)



PCI Configuration Address Offset
04h

SROM Offset
NA

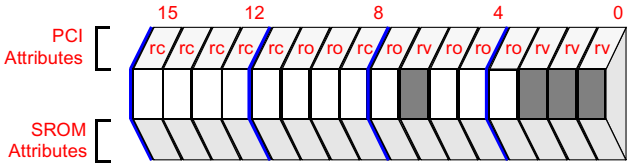
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
04	0b	Memory Write and Invalidate Enable (MWIE): the 31154 Bridge does not promote MW transactions to MWI transactions. MWI transactions targeting resources on the opposite side of the bridge, however, are forwarded as MWI transactions.
03	0b	Special Cycle Enable (SCE): the 31154 Bridge ignores special cycle transactions. This bit is read only and always returns 0 when read.
02	0b	Bus Master Enable (BME): Enables the 31154 Bridge to initiate memory and I/O transactions on the primary interface. Initiation of configuration transactions is not affected by the state of this bit. 0 = the 31154 Bridge will not initiate memory or I/O transactions on the primary interface. 1 = the 31154 Bridge is enabled to function as an initiator on the primary interface.
01	0b	Memory Space Enable (MSE): Controls target response to memory transactions on the primary interface. 0 = the 31154 Bridge target response to memory transactions on the primary interface is disabled. 1 = the 31154 Bridge target response to memory transactions on the primary interface is enabled.
00	0b	I/O Space Enable (IOSE): Controls target response to I/O transactions on the primary interface. 0 = the 31154 Bridge target response to I/O transactions on the primary interface is disabled. 1 = the 31154 Bridge target response to I/O transactions on the primary interface is enabled.

5.1.3 Offset 06H: PSTS - Primary Status

Bits in this register are either Read Only (RO) or Read, Write Clear (RWC).

Table 40. PSTS - Primary Status (Sheet 1 of 2)



PCI Configuration Address Offset
06h

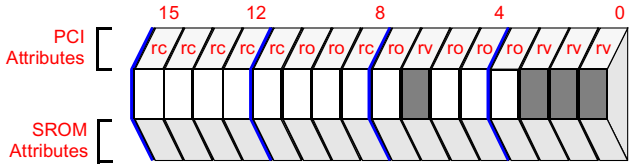
SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only

RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15	0b	Detected Parity Error: the 31154 Bridge sets this bit to a 1b whenever it detects an address, attribute or data parity error. This bit is set regardless of the state of the PER bit in the command register.
14	0b	Signaled System Error: the 31154 Bridge sets this bit to a 1b whenever it asserts SERR# on the primary bus.
13	0b	Received Master Abort: the 31154 Bridge sets this bit to a 1b when, acting as the initiator on the primary bus, its transaction (with the exception of special cycles) has been terminated with a Master Abort.
12	0b	Received Target Abort: the 31154 Bridge sets this bit to a 1b when, acting as the initiator on the primary bus, its transaction has been terminated with a Target Abort.
11	0b	Signaled Target Abort: the 31154 Bridge sets this bit to a 1b when it, as the target of a transaction, terminates it with a Target Abort. In PCI-X mode this bit is also set when it forwards a SCM with a target abort error code.
10:09	01b	DEVSEL# Timing: Indicates slowest response to a non-configuration command on the primary interface. Returns “01b” when read, indicating that the 31154 Bridge responds no slower than with medium timing.
08	0b	Master Data Parity Error: the 31154 Bridge sets this bit to a 1b when all of the following conditions are true: • the 31154 Bridge is the current master on the primary bus. • P_PERR# is detected asserted or is asserted by the 31154 Bridge. • The Parity Error Response bit is set in the Command register.
07	1b	Fast Back to Back Capable: Returns a 1b when read indicating that the 31154 Bridge is able to respond to fast back to back transactions on its primary interface.
06	0b	Reserved.
05	1b	66 MHz Capable Indication: Returns a 1b when read indicating that the 31154 Bridge primary interface is 66 MHz capable.

Table 40. PSTS - Primary Status (Sheet 2 of 2)



PCI Configuration Address Offset
06h

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

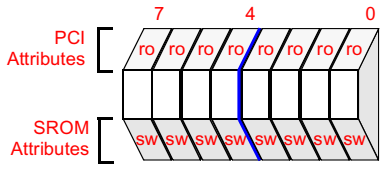
Bit	Default	Description
04	1b	Capabilities List Enable: Returns 1b when read indicating that the 31154 Bridge supports PCI standard enhanced capabilities. Offset 34h (Capability Pointer register) provides the offset for the first entry in the linked list of enhanced capabilities.
03	0b	Interrupt Status the 31154 Bridge does not generate interrupts. This bit will always return 0b on reads.
02:00	0h	Reserved.

5.1.4 Offset 08H: RID - Revision ID

Revision ID Register.

This register is pre-loadable by setting offset 00h of the Serial ROM to 1000_0001b.

Table 41. RID - Revision ID



PCI Configuration Address Offset
08h

SROM Offset
28h

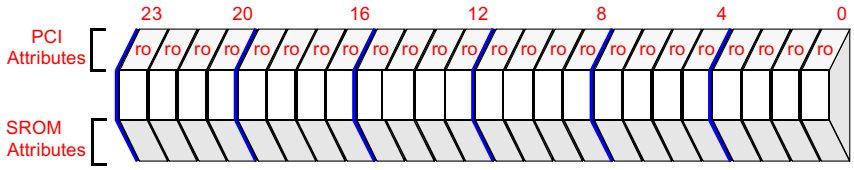
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	00h	Revision ID (RID): '00h' indicating the 31154 Bridge A-0 stepping.

5.1.5 Offset 09H: CC - Class Code

This contains the class code, sub class code, and programming interface for the device.

Table 42. CC - Class Code



PCI Configuration Address Offset
09h

SROM Offset
NA

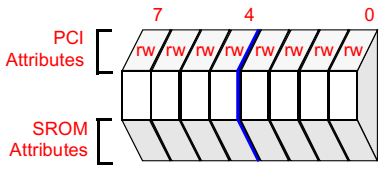
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
23:16	06h	Base Class Code (BCC): Indicates that this is a bridge device.
15:08	04h	Sub Class Code (SCC): Indicates this is of type PCI-to-PCI bridge.
07:00	00h	Programming Interface (PIF): Indicates that this is standard (non-subtractive) PCI-PCI bridge.

5.1.6 Offset 0CH: CLS - Cache Line Size

This indicates the cache line size of the host system.

Table 43. CLS - Cache Line Size



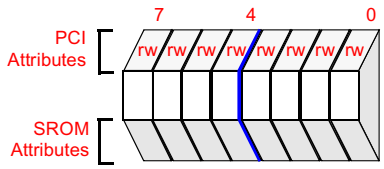
PCI Configuration Address Offset	SROM Offset	Attribute Legend:	
0Ch	NA	RV = Reserved RW = Read/Write RO = Read Only	RT = Read/Toggle RC = Read/Clear SW = SROM Write NA = Not Accessible

Bit	Default	Description
07:00	00h	Cache Line Size (CLS): Designates the cache line size in 32-bit dword units. The contents of this register are factored into internal policy decisions associated with memory read prefetching. Valid cache line sizes are 8 and 16dwords. If the cache line size is set to an invalid value, the 31154 Bridge behaves as though the cache line size was set to 00h.

5.1.7 Offset 0DH: PLT - Primary Latency Timer

Primary bus MLT.

Table 44. PLT - Primary Latency Timer



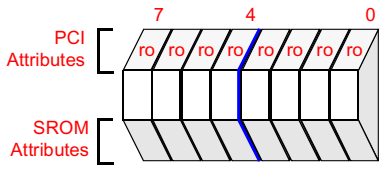
PCI Configuration Address Offset	SROM Offset	Attribute Legend:	
0Dh	NA	RV = Reserved RW = Read/Write RO = Read Only	RT = Read/Toggle RC = Read/Clear SW = SROM Write NA = Not Accessible

Bit	Default	Description
07:00	00h Conventional PCI -or- 40h PCI-X	Primary Latency Timer (PTV): Conventional PCI Mode: Primary bus Master latency timer. Indicates the number of PCI clock cycles, referenced from the assertion of FRAME# to the expiration of the timer, when the 31154 Bridge may continue as master of the current transaction. All bits are writeable, resulting in a granularity of 1 PCI clock cycle. When the timer expires (i.e., equals 00h) the 31154 Bridge relinquishes the bus after the first data transfer when its PCI bus grant has been deasserted. PCI-X Mode: Primary bus Master latency timer. Indicates the number of PCI clock cycles, referenced from the assertion of FRAME# to the expiration of the timer, when the 31154 Bridge may continue as master of the current transaction. All bits are writeable, resulting in a granularity of 1 PCI clock cycle. When the timer expires (i.e., equals 00h) the 31154 Bridge relinquishes the bus at the next ADB. (Except in the case where MLT expires within 3 data phases of an ADB. In this case the 31154 Bridge will complete the current ADB and continue on until it reaches the next ADB before relinquishing the bus)

5.1.8 Offset 0EH: HTYPE - Header Type

This register indicates the 31154 Bridge PCI Configuration Header Type. The 31154 Bridge reports that it is a single function (i.e., not a multi-function device), and that its PCI header type conforms to the PCI standard Type 1 header layout.

Table 45. HTYPE - Header Type



PCI Configuration Address Offset
0Eh

SROM Offset
NA

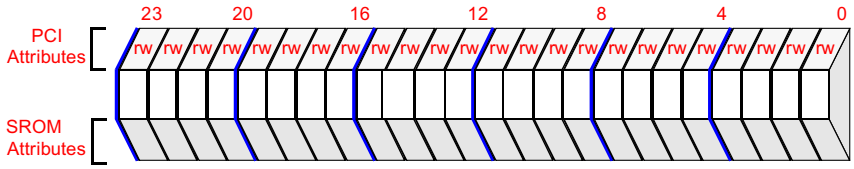
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07	0b	Multi-function device (MFD): Returns '0b' when read indicating that the bridge is a single function device.
06:00	01h	Header Type (HTYPE): Defines the layout of addresses 10h through 3Fh in configuration space. Returns “01h” when read indicating that the register layout conforms to the standard PCI-to-PCI bridge layout.

5.1.9 Offset 18H: BNUM - Bus Number Register

This register is used to configure the 31154 Bridge primary, secondary, and maximum subordinate bus numbers.

Table 46. BNUM - Bus Number Register



PCI Configuration Address Offset: 18h

SROM Offset: NA

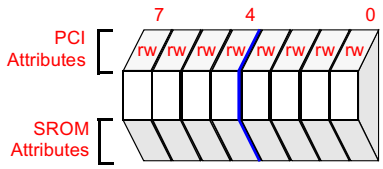
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
23:16	00h	Subordinate Bus Number (SBBN): Indicates the highest PCI bus number below this bridge. Any Type 1 configuration cycle on the primary bus whose bus number is greater than the secondary bus number, and less than or equal to the subordinate bus number will be forwarded unaltered as a Type 1 configuration cycle on the secondary PCI bus.
15:08	00h	Secondary Bus Number (SCBN): Indicates the bus number of PCI to which the secondary interface is connected. Any Type 1 configuration cycle matching this bus number will be translated to a Type 0 configuration cycle (or a Special Cycle) before being executed on the the 31154 Bridge's secondary PCI bus.
07:00	00h	Primary Bus Number (PBN): Indicates the the 31154 Bridge primary bus number. Any Type 1 configuration cycle on the primary interface with a bus number that is less than the contents of this register field will not be claimed by the 31154 Bridge.

5.1.10 Offset 1BH: SLT - Secondary Latency Timer

Secondary MLT.

Table 47. SLT - Secondary Latency Timer



PCI Configuration Address Offset	SROM Offset	Attribute Legend:	
1Bh	NA	RV = Reserved RW = Read/Write RO = Read Only	RT = Read/Toggle RC = Read/Clear SW = SROM Write NA = Not Accessible

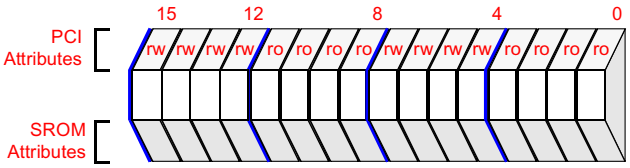
Bit	Default	Description
07:00	00h Conventional PCI -or- 40h PCI-X	Secondary Latency Timer (STV): Conventional PCI Mode: Secondary bus Master latency timer. Indicates the number of PCI clock cycles, referenced from the assertion of FRAME# to the expiration of the timer, when the 31154 Bridge may continue as master of the current transaction. All bits are writeable, resulting in a granularity of 1 PCI clock cycle. When the timer expires (i.e., equals 00h) the 31154 Bridge relinquishes the bus after the first data transfer when its PCI bus grant has been deasserted. PCI-X Mode: Secondary bus Master latency timer. Indicates the number of PCI clock cycles, referenced from the assertion of FRAME# to the expiration of the timer, when the 31154 Bridge may continue as master of the current transaction. All bits are writeable, resulting in a granularity of 1 PCI clock cycle. When the timer expires (i.e., equals 00h) the 31154 Bridge relinquishes the bus at the next ADB. (Except in the case where MLT expires within 3 data phases of an ADB. In this case the 31154 Bridge will complete the current ADB and continue on until it reaches the next ADB before relinquishing the bus)

5.1.11 Offset 1CH: IOBL - I/O Base and Limit Register

This register defines, by way of base and limit fields, a 4K Byte aligned address range. I/O transactions originating on the 31154 Bridge primary bus that address an I/O location falling within the range specified in this register are subsequently forwarded to the 31154 Bridge secondary PCI bus[1].

I/O transactions on the primary bus that address an I/O location that is outside of the range specified by the contents of this register will not be forwarded by the 31154 Bridge[2].

Table 48. IOBL - I/O Base and Limit Register



PCI Configuration Address Offset
1Ch

SROM Offset
NA

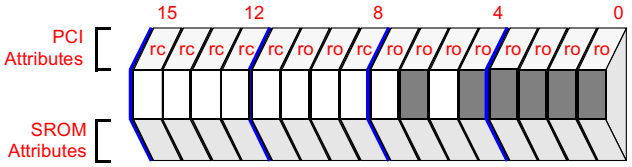
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:12	0h	I/O Limit Address Bits [15:12]: Defines the top address of an address range to determine when to forward I/O transactions from one interface to the other. These bits correspond to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be FFFh.
11:08	1h	I/O Limit Addressing Capability: This field is hard-wired to 1h, indicating support 32-bit I/O addressing.
07:04	0h	I/O Base Address Bits [15:12]: Defines the bottom address of an address range to determine when to forward I/O transactions from one interface to the other. These bits correspond to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be 000h.
03:00	1h	I/O Base Addressing Capability: This is hard-wired to 1h, indicating support for 32-bit I/O addressing.

1. Provided that the I/O Space Enable bit of the PCI Command register is set.
2. With the exception of legacy I/O transactions if enabled (e.g., VGA palette snoops).

5.1.12 Offset 1EH: SSTS - Secondary Status Register

Table 49. SSTS - Secondary Status Register



PCI Configuration Address Offset
1Eh

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15	0b	Detected Parity Error: the 31154 Bridge sets this bit to a 1b whenever it detects an address, attribute or data parity error on its secondary interface.
14	0b	Received System Error: the 31154 Bridge sets this bit if it samples SERR# asserted on its secondary bus interface.
13	0b	Received Master Abort: the 31154 Bridge sets this bit to a 1b when, acting as the initiator on the secondary bus, it's transaction (with the exception of special cycles) has been terminated with a Master Abort.
12	0b	Received Target Abort: the 31154 Bridge sets this bit to a 1b when, acting as the initiator on the secondary bus, it's transaction has been terminated with a Target Abort.
11	0b	Signaled Target Abort: the 31154 Bridge sets this bit to a 1b when it, as the target of a transaction, terminates it with a Target Abort. In PCI-X mode this bit is also set when it forwards a SCM with a target abort error code.
10:09	01b	DEVSEL# Timing: Indicates slowest response to a non-configuration command on the secondary interface. Returns “01b” when read, indicating that the 31154 Bridge responds no slower than with medium timing.
08	0b	Master Data Parity Error: the 31154 Bridge sets this bit to a 1b when all of the following conditions are true: • the 31154 Bridge is the current master on the secondary bus. • S_PERR# is detected asserted or is asserted by the 31154 Bridge. • The Parity Error Response bit is set in the Command register.
07	1b	Fast Back-to-Back Capable (FBC):Indicates that the secondary interface of the 31154 Bridge can receive fast back-to-back cycles.
06	0b	Reserved.
05	1b	66 MHz Capable (C66): Indicates the secondary interface of the bridge is 66 MHz capable.
04:00	00h	Reserved.

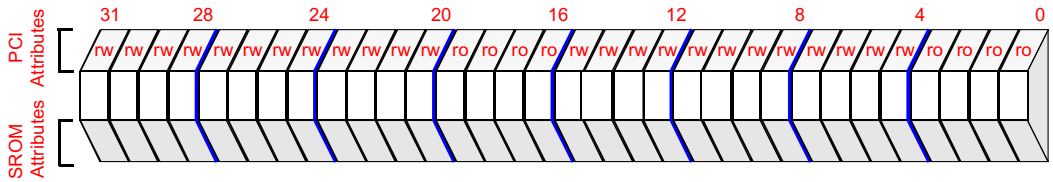
5.1.13 Offset 20H: MBL - Memory Base and Limit Register

This register defines, by way of base and limit fields, the memory mapped I/O address range that is claimed on the primary interface and forwarded to the bridges secondary PCI bus.

Memory transactions originating on the the 31154 Bridge primary bus that address a memory location falling within the range specified by this register are subsequently forwarded to the 31154 Bridge secondary PCI bus[1]

A memory transaction, whose address is within the address range specified by this register is treated as a non-prefetchable transaction. The non-prefetchable memory address window is typically used for accessing memory mapped I/O locations where read side-affects may occur.

Table 50. MBL - Memory Base and Limit Register



PCI Configuration Address Offset
20h

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:20	000h	Memory Limit: These 12 bits are compared with P_AD[31:20] of the incoming address to determine the upper 1MB aligned value (exclusive) of the range. The incoming address must be less than or equal to this value. For the purposes of address decoding the lower 20 address bits (P_AD[19:0]) are assumed to be F FFFFh.
19:16	0h	Reserved.
15:04	000h	Memory Base: These 12 bits are compared with bits P_AD[31:20] of the incoming address to determine the lower 1MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value. For the purposes of address decoding the lower 20 address bits (P_AD[19:0]) are assumed to be 0 0000h.
03:00	0h	Reserved.

1. .Provided that the Memory Space Enable bit of the PCI Command register is set.

5.1.14 Offset 24H: PMBL - Prefetchable Memory Base and Limit Register

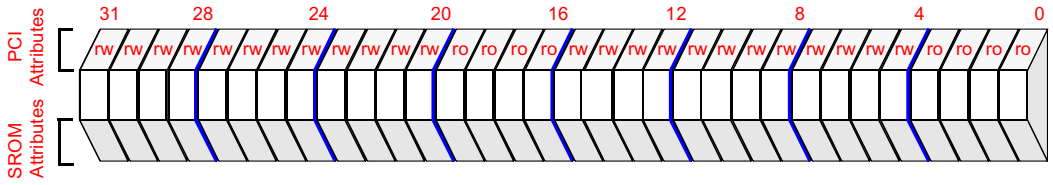
This register defines, by way of base and limit fields, the memory mapped I/O address range that is claimed on the primary interface and forwarded to the bridges secondary PCI bus.

Memory transactions originating on the the 31154 Bridge primary bus that address a memory location falling within the range specified by this register are subsequently forwarded to the 31154 Bridge secondary PCI bus[1].

A memory transaction, whose address is within the address range specified by this register is treated as a prefetchable transaction. The prefetchable memory address window must only be used for accessing memory locations where there are no read side-affects.

The guarantee of no read side affects enables the bridge to speculatively prefetch additional read data in anticipation of its being requested shortly thereafter.

Table 51. PMBL - Prefetchable Memory Base and Limit Register



PCI Configuration Address Offset
24h

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

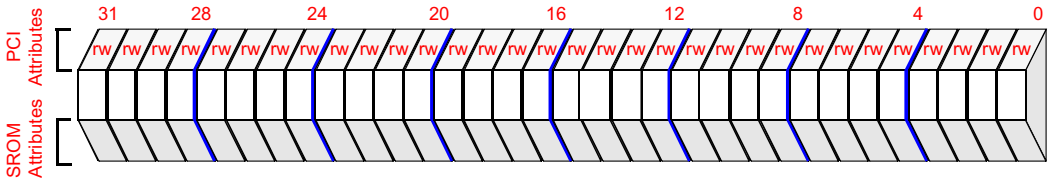
Bit	Default	Description
31:20	000h	Prefetchable Memory Limit: These 12 bits are compared with P_AD[31:20] of the incoming address to determine the upper 1MB aligned value (exclusive) of the range. The incoming address must be less than or equal to this value. For the purposes of address decoding the lower 20 address bits (P_AD[19:0]) are assumed to be F FFFFh.
19:16	1h	64-bit Indicator: Indicates that 64-bit addressing is supported.
15:04	000h	Prefetchable Memory Base: These 12 bits are compared with bits P_AD[31:20] of the incoming address to determine the lower 1MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value. For the purposes of address decoding the lower 20 address bits (P_AD[19:0]) are assumed to be 0 0000h.
03:00	1h	64-bit Indicator: Indicates that 64-bit addressing is supported.

1. Provided that the Memory Space Enable bit of the PCI Command register is set.

5.1.15 Offset 28H: PMBU32 - Prefetchable Memory Base Upper 32 Bits

This defines the upper 32 bits of the prefetchable address base register.

Table 52. PMBU32 - Prefetchable Memory Base Upper 32 Bits



PCI Configuration Address Offset
28h

SROM Offset
NA

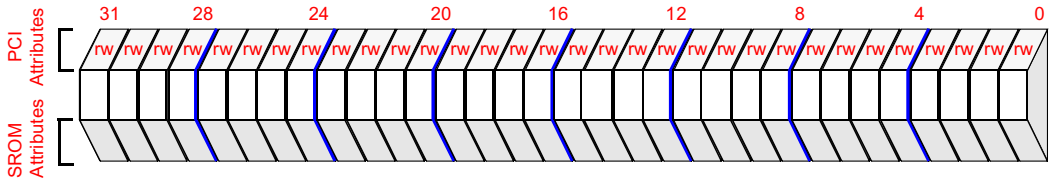
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:00	00000000h	Prefetchable Memory Base Upper Portion: All bits are read/writeable - the 31154 Bridge supports full 64-bit addressing.

5.1.16 Offset 2CH: PMLU32 - Prefetchable Memory Limit Upper 32 Bits

This defines the upper 32 bits of the prefetchable address limit register.

Table 53. PMBU32 - Prefetchable Memory Base Upper 32 Bits



PCI Configuration Address Offset
2Ch

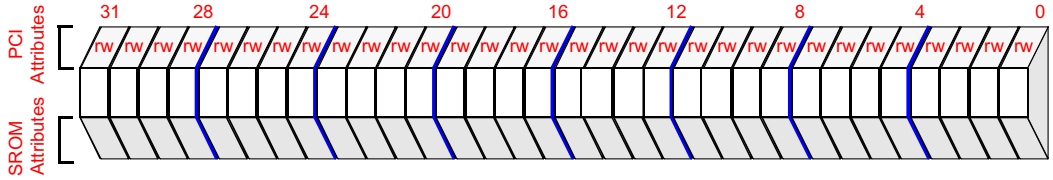
SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:00	00000000h	Prefetchable Memory Limit Upper 32 Bits: All bits are read/writeable - the 31154 Bridge supports full 64-bit addressing.

5.1.17 Offset 30H: IOBLU16 - I/O Base and Limit Upper 16 Bits

Table 54. IOBLU16 - I/O Base and Limit Upper 16 Bits



PCI Configuration Address Offset
30h

SROM Offset
NA

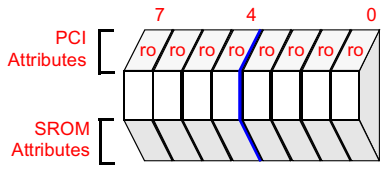
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:16	0000h	I/O Limit High 16 Bits: Upper 16 address lines (AD(31:16) used in conjunction with the I/O Limit Register (offset 1Dh) to construct the 32-bit I/O limit address.
15:00	0000h	I/O Base High 16 Bits: Upper 16 address lines (AD(31:16) used in conjunction with the I/O Base Register (offset 1Ch) to construct the 32-bit I/O base address.

5.1.18 Offset 34H: CAPP - Capabilities List Pointer

Contains the pointer to the first entry in the capabilities list.

Table 55. CAPP - Capabilities List Pointer



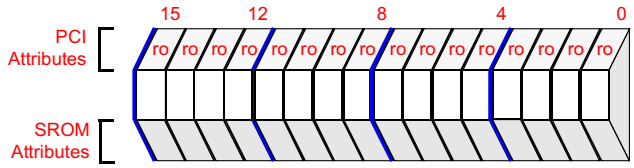
PCI Configuration Address Offset	SROM Offset	Attribute Legend:	
34h	NA	RV = Reserved RW = Read/Write RO = Read Only	RT = Read/Toggle RC = Read/Clear SW = SROM Write NA = Not Accessible

Bit	Default	Description
07:00	D4h	Capabilities Pointer: Pointer to the first CAP ID entry in the capabilities list is at D4h in PCI configuration space. (PCI Chassis / Slot Registers)

5.1.19 Offset 3CH: INTR - Interrupt Information

This register contains information on interrupts and while required is not utilized by PCI-to-PCI bridges.

Table 56. INTR - Interrupt Information



PCI Configuration Address Offset
3Ch

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

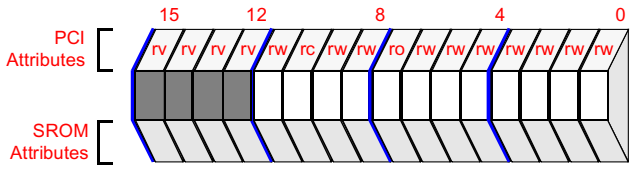
Bit	Default	Description
15:08	00h	Interrupt Pin (PIN): Bridges do not support the generation of interrupts.
07:00	00h	Interrupt Line (LINE): the 31154 Bridge Bridge does not generate interrupts, so this is reserved as '00h'.

5.1.20 Offset 3EH: BCTRL - Bridge Control Register

This register provides extensions to the Command register that are specific to a PCI-to-PCI bridge. The Bridge Control register provides many of the same controls for the secondary interface that are provided by the Command register for the primary interface.

Some bits affect operation of both interfaces of a bridge.

Table 57. BCTRL - Bridge Control Register (Sheet 1 of 3)



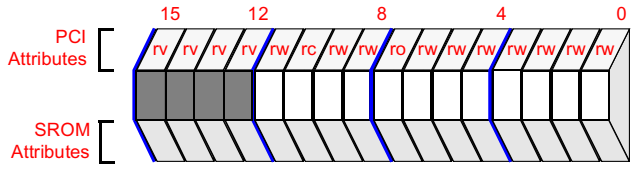
PCI Configuration Address Offset
3Eh

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:12	0h	Reserved
11	0b	Discard Timer SERR# Enable: Controls the generation of SERR# on the primary interface (P_SERR#) in response to a timer discard on either the primary or secondary interface. 0b = SERR# is not asserted. 1b = SERR# is asserted.
10	0b	Discard Timer Status (DTS): This bit is set to a '1b' when either the primary or secondary discard timer expires. The delayed completion is then discarded.
09	0b	Secondary Discard Timer (SDT): Sets the maximum number of PCI clock cycles that the 31154 Bridge waits for an initiator on the secondary bus to repeat a delayed transaction request. The counter starts when the delayed transaction completion is ready to be returned to the initiator. If the initiator has not repeated the transaction at least once before the counter expires, the 31154 Bridge discards the delayed transaction from its queues. 0b = The secondary master time-out counter is 2^{15} PCI clock cycles. 1b = The secondary master time-out counter is 2^{10} PCI clock cycles.
80	0b	Primary Discard Timer (PDT): Sets the maximum number of PCI clock cycles that the 31154 Bridge waits for an initiator on the primary bus to repeat a delayed transaction request. The counter starts when the delayed transaction completion is ready to be returned to the initiator. If the initiator has not repeated the transaction at least once before the counter expires, the 31154 Bridge discards the delayed transaction from its queues. 0b = The primary master time-out counter is 2^{15} PCI clock cycles. 1b = The primary master time-out counter is 2^{10} PCI clock cycles.
07	0b	Fast Back-to-Back Enable (FBE): the 31154 Bridge does not initiate back to back transactions.
06	0b	Secondary Bus Reset (SBR): When cleared to 0b: the 31154 Bridge deasserts S_RST#, if it had been asserted by writing this bit to a 1b. When set to 1b: the 31154 Bridge asserts S_RST#.

Table 57. BCTRL - Bridge Control Register (Sheet 2 of 3)



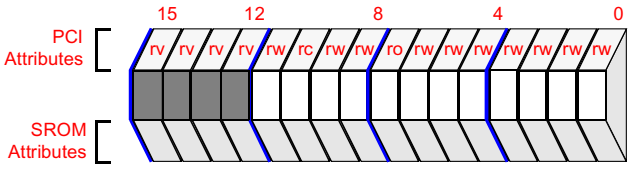
PCI Configuration Address Offset
3Eh

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
05	0b	Master Abort Mode (MAM): Dictates the 31154 Bridge behavior on the initiator bus when a master abort termination occurs in response to a delayed transaction initiated by the 31154 Bridge on the target bus. 0b = the 31154 Bridge asserts TRDY# in response to a non-locked delayed transaction, and returns FFFF FFFFh if a read. See Section 3.13, “PCI-X Bus Mode” on page 64 for response to locked transactions. 1b = If the transaction had not yet been completed on the initiator bus (e.g., delayed reads, or non-posted writes), then the 31154 Bridge returns a Target Abort in response to the original requester when it returns looking for its delayed completion on the initiator bus. If the transaction had completed on the initiator bus (e.g., a PMW), then the 31154 Bridge asserts P_SERR# (if enabled). For PCI-X transactions this bit is an enable for the assertion of P_SERR# due to a master abort while attempting to deliver a posted memory write on the destination bus.
04	0b	VGA Alias Filter Enable: This bit dictates bridge behavior in conjunction with the VGA enable bit (also of this register), and the VGA Palette Snoop Enable bit (Command Register). If the VGA enable, or VGA Palette Snoop enable bits are on (i.e., 1b) the VGA Aliasing bit will, for the corresponding enabled functionality: 0b = Ignore address bits AD[15:10] when decoding VGA I/O addresses. 1b = Ensure that address bits AD[15:10] equal 000000b when decoding VGA I/O addresses. If all VGA cycle forwarding is disabled, (i.e., VGA Enable bit =0b and VGA Palette Snoop bit =0b), then this bit has no impact on bridge behavior.
03	0b	VGA Enable: Setting this bit enables address decoding and transaction forwarding of the following VGA transactions from the primary bus to the secondary bus: • frame buffer memory addresses 000A0000h:000BFFFFh· • VGA I/O addresses 3B0:3BBh and 3C0h:3DFh, where AD[31:16] = “0000h” and AD[15:10] are either not decoded (i.e., don't cares), or must be “000000b” depending upon the state of the VGA Alias Filter Enable bit. (bit(4) of this register). I/O and Memory Enable bits must be set in the Command register to enable forwarding of VGA cycles.

Table 57. BCTRL - Bridge Control Register (Sheet 3 of 3)



PCI Configuration Address Offset
3Eh

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
02	0b	ISA Enable: Setting this bit enables special handling for the forwarding of ISA I/O transactions that fall within the address range specified by the I/O Base and Limit registers, and are within the lowest 64Kbyte of the I/O address map (i.e., 0000 0000h - 0000 FFFFh). 0b = All I/O transactions that fall within the I/O Base and Limit registers' specified range are forwarded from primary to secondary unfiltered. 1b = Blocks the forwarding from primary to secondary of the top 768 bytes of each 1Kbyte alias. On the secondary the top 768 bytes of each 1K alias are inversely decoded and forwarded from secondary to primary.
01	0b	SERR# Forward Enable: 0b = the 31154 Bridge does not assert P_SERR# as a result of an S_SERR# assertion. 1b = the 31154 Bridge asserts P_SERR# whenever S_SERR# is detected asserted provided the SERR# Enable bit is set (PCI Command Register bit(8)=1b).
00	0b	Parity Error Response: This bit controls the 31154 Bridge response to a parity error that is detected on its secondary interface. 0b = If a data parity error is detected the 31154 Bridge does not assert P_PERR#. Also the 31154 Bridge does not assert P_SERR# in response to a detected address or attribute parity error. 1b = If a data parity error is detected the 31154 Bridge asserts P_PERR#. the 31154 Bridge also asserts P_SERR# (if enabled globally via bit(8) of the Command register) in response to a detected address or attribute parity error.

5.2 Device Specific Registers

The following sections provide detail on the programming interface for the 31154 Bridge device specific registers. These registers reside in the 31154 Bridge PCI configuration address space with an offset range of 40h - CBh.

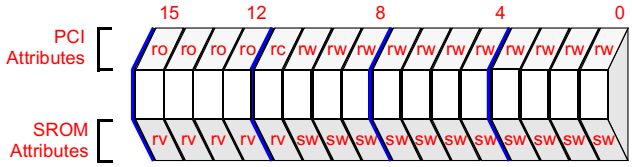
Table 58. 31154 Bridge Device-Specific Configuration Address Map

Byte 3	Byte 2	Byte 1	Byte 0	Configuration Byte Offset
Bridge Control 0ψ	Arbiter Control/Statusψ		Reserved	40h
Bridge Control 2ψ		Bridge Control 1ψ		44h
Serial Prom address		Bridge Status		48h
Serial Prom data				4Ch
Prefetch Policyψ		Multi-Transaction Timerψ		50h
Misc. Pin Status	Pre-boot Status	P_SERR# Assertion Controlψ		54h
Reserved				58h
Secondary IDSEL Function 0 Enableψ		Secondary IDSELψ		5Ch
Reserved				60h
Reserved				64h
Reserved	GPIO Pin Status	GPIO W1TT Dataψ	GPIO Pin Configurationψ	68h
Opaque Memory Base and Limitψ				6Ch
Opaque Memory Base Upper 32 Bitsψ				70h
Opaque Memory Limit Upper 32 Bitsψ				74h
Reserved				78h:D3h

Note: Registers named in Table 58 that are suffixed with a ψ symbol, may be pre-loaded using the serial ROM interface.

5.2.1 Offset 41H: ARB_CSR - Secondary Arbiter Control /Status Register

Table 59. ARB_CSR - Secondary Arbiter Control/Status Register (Sheet 1 of 2)



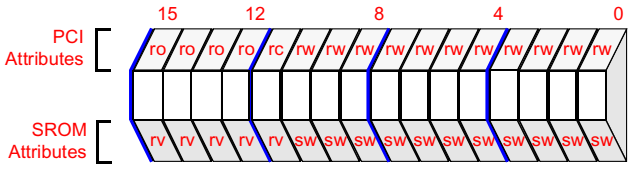
PCI Configuration Address Offset
41h

SROM Offset
01h

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:12	1111b	Grant Time-out Violator: This field indicates the agent that violated the Grant Time-out rule (PCI = 16 clocks, PCI-X = 6 clocks). Note that this field is only meaningful if: • Bit[11] of this register is set to 1b, indicating that a Grant Time-out violation had occurred. • the 31154 Bridge internal arbiter is enabled. Bits[15:12] Violating Agent (REQ#/GNT# pair number) 0000b REQ#/GNT#[0] 0001b REQ#/GNT#[1] . . . . . . 1111b Default Value (no violation detected) When bit[11] is cleared by software, this field reverts back to its default value.
11	0b	Grant Time-out Occurred: When set to 1b, this indicates that a Grant Time-out error had occurred involving one of the secondary bus agents. Software clears this bit by writing a 1b to it.

Table 59. ARB_CSR - Secondary Arbiter Control/Status Register (Sheet 2 of 2)



PCI Configuration Address Offset
41h

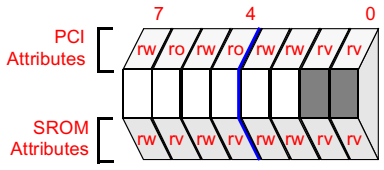
SROM Offset
01h

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
10	1b	Bus Parking Control: 0b = During bus idle, the 31154 Bridge parks the bus on the last master to use the bus. 1b = During bus idle, the 31154 Bridge parks the bus on itself. The bus grant is removed from the last master and internally asserted to the 31154 Bridge.
09:00	10 0000 0000b	Secondary Bus Arbiter Priority Configuration: the 31154 Bridge secondary arbiter provides two rings of arbitration priority. Each bit of this field assigns its corresponding secondary bus master to either the high priority arbiter ring (1b) or to the low priority arbiter ring (0b). Bits [8:0] correspond to request inputs S_REQ#[8:0], respectively. Bit [9] corresponds to the the 31154 Bridge internal secondary bus request. 0b = Indicates that the master belongs to the low priority group. 1b = Indicates that the master belongs to the high priority group. **NOTE:** Refer to Section 4.3, “Conventional PCI Arbitration” on page 74 for description of the two-tiered arbitration scheme.
00	0	REQ0# Arbiter Priority / Component Reset When the Component Reset Enable (CRSTEN) pin is asserted, this bit provides component reset control. Otherwise it acts as the arbiter priority for REQ0#. **REQ0# Arbiter Control** 0b = Indicates that the master belongs to the low priority group. 1b = Indicates that the master belongs to the high priority group. **Component Reset** When asserted, the bridge performs a full chip reset. Data buffers, configuration registers, and the scondary interface are reset to thier initial state. SROM Preload is performed Secondary bus reset S_RST# is asserted for a minimum of 1ms to enforce the T_{rst} requirement. This bit is self clearing and will return to ‘0’ once the reset is complete. ***Warning:*** If utilizing the component reset, this bit should never be set by the SROM preload as an infinite loop will result.

5.2.2 Offset 43H: VCR0 - the 31154 Bridge Control Register 0

Table 60. VCR0 - 31154 Bridge Control Register 0 (Sheet 1 of 2)



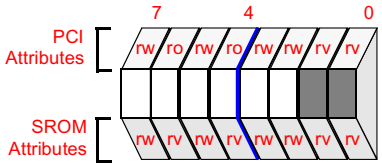
PCI Configuration Address Offset
43h

SROM Offset
03h

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07	0b	Fully Dynamic Queue When set '1' the bridge will operate in fully dynamic queue mode. The bridge will enqueuq up to 14 PMY transactions and 8KB of posted data. When '0', the bridge will limit the number of Posted Write transactions to 8 and limit write data to 4KB. **NOTE:** When enabled, no space is reserved for Read Requests and Split Completions..
06	0b	Queues Empty: 0b = Indicates that there are pending transactions resident on the bridge. 1b = Indicates that all of the the 31154 Bridge queues (request and data) are empty. Once set this bit is automatically cleared when software clears (writes 0b) to the New Transaction Mask bit. **NOTE:** This bit is only valid in response to buffer flushing initiated by setting the New Transaction Mask bit of this register.
05	0b	New Transactions Mask: This bit is used to dynamically disable the 31154 Bridge ability to enqueue any new transactions. Transactions currently enqueued within the 31154 Bridge at the time that transaction queuing is disabled using this mechanism are completed normally. 0b = the 31154 Bridge behaves normally. 1b = the 31154 Bridge reacts to new transaction requests on either bus interface as through there was no free request queue space (i.e., the transaction is not enqueued, and the requester is retried). the 31154 Bridge PCI Configuration registers are visible to host software, regardless of the state of this bit. The combination of this bit and the QE bit enables applications, via program control, to purge the 31154 Bridge currently pending transactions.
04	0b	Invalidate Complete: This bit indicates that the 31154 Bridge has invalidated all of its request and data queues (in both directions). 0b = Invalidation operation is in process.. 1b = Invalidation operation has completed. **NOTE:** Note that this bit is only valid in response to an Invalidate Queues operation, initiated by setting the Invalidate Queues bit of this register.

Table 60. VCR0 - 31154 Bridge Control Register 0 (Sheet 2 of 2)



PCI Configuration Address Offset
43h

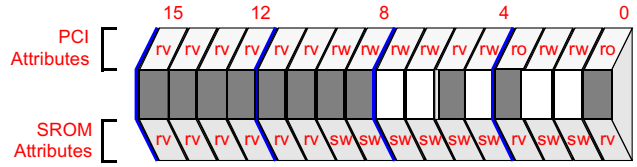
SROM Offset
03h

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
03	0b	Invalidate Queues: This bit is used to invalidate all internal requests and data currently residing within the 31154 Bridge. 0b = the 31154 Bridge behaves normally. 1b = the 31154 Bridge invalidates all request queues and data buffers.Software sets this bit to execute the Invalidate Queues operation, and then polls the Invalidate Complete bit, also of this register, to determine when the operation has been completed.
02	0b	Upstream Prefetch Disable: This bit disables the 31154 Bridge ability to perform upstream prefetch operations for Memory Read requests received on its secondary interface. This bit also controls the bridge's ability to generate advanced read commands when forwarding a Memory Read Block transaction request upstream from a PCI-X bus to a Conventional PCI bus. 0b = the 31154 Bridge treats all upstream Memory Read requests as if they target prefetchable memory. The use of Memory Read Line and Memory Read Multiple is enabled when forwarding a PCI-X Memory Read Block request to an upstream bus operating in Conventional PCI mode. 1b = the 31154 Bridge treats upstream PCI Memory Read requests as if they target non-prefetchable memory and forwards upstream PCI-X Memory Read Block commands as Memory Read when the primary bus is operating in Conventional PCI mode. **NOTE:** This bit does not affect the 31154 Bridge ability to perform read prefetching if the received command is Memory Read Line or Memory Read Multiple.
01:00	00b	Reserved.

5.2.3 Offset 44H: VCR1 - 31154 Bridge Control Register 1

Table 61. VCR1 - 31154 Bridge Control Register 1 (Sheet 1 of 2)



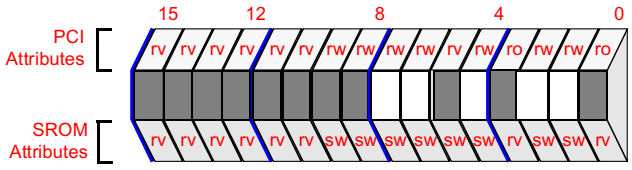
PCI Configuration Address Offset
44h

SROM Offset
04h

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:08	0000000b	Reserved
07:06	00b	Alias Command Mapping: This two bit field determines how the 31154 Bridge handles PCI-X “Alias” commands, specifically the Alias to Memory Read Block and Alias to Memory Write Block commands. The three options for handling these alias commands are to either pass it as is, re-map to the actual block memory read/write command encoding, or ignore the transaction forcing a Master Abort to occur on the Origination Bus. Bit (7:6) — Handling of command 0 0 — Re-map to Memory Read/Write Block before forwarding. 0 1 — Enqueue and forward the alias command code unaltered. 1 0 — Ignore the transaction, forcing Master Abort. 1 1 — Reserved.
05	1b	Reserved: Software must always write a 1 to this bit.
04	1b	GRANT# time-out disable: This bit enables/disables the GNT# time-out mechanism. Grant time-out is 16 clocks for Conventional PCI, and six clocks for PCI-X. 0b = The Secondary bus arbiter will time out an agent that does not assert FRAME# within 16/6 clocks of receiving its grant, once the bus has gone idle. The time-out counter begins as soon as the bus goes idle with the new GNT# asserted. An infringing agent will not receive a subsequent GNT# until it de-asserts its REQ# for at least one clock cycle. 1b = GNT# time-out mechanism is disabled.
03	0b	Reserved.

Table 61. VCR1 - 31154 Bridge Control Register 1 (Sheet 2 of 2)



PCI Configuration Address Offset
44h

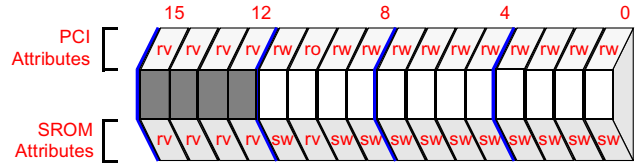
SROM Offset
04h

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
02	0b	Secondary Discard Timer Disable: This bit enables/disables the 31154 Bridge secondary delayed transaction discard mechanism. The time out mechanism is used to ensure that initiators of delayed transactions return for their delayed completion data/status within a reasonable amount of time after it is available from the 31154 Bridge. 0b = The secondary master time-out counter is enabled and uses the value specified by the Secondary Discard Timer bit (see Bridge Control Register). 1b = The secondary master time-out counter is disabled. the 31154 Bridge waits indefinitely for a secondary bus master to repeat a delayed transaction.
01	0b	Primary Discard Timer Disable: This bit enables/disables the 31154 Bridge primary delayed transaction discard mechanism. The time out mechanism is used to ensure that initiators of delayed transactions return for their delayed completion data/status within a reasonable amount of time after it is available from the 31154 Bridge. 0b = The primary master time-out counter is enabled and uses the value specified by the Primary Discard Timer bit (see Bridge Control Register). 1b = The secondary master time-out counter is disabled. the 31154 Bridge waits indefinitely for a secondary bus master to repeat a delayed transaction.
00	0b	Reserved.

5.2.4 Offset 46H: VCR2 - 31154 Bridge Control Register 2

Table 62. VCR2 - 31154 Bridge Control Register 2 (Sheet 1 of 2)



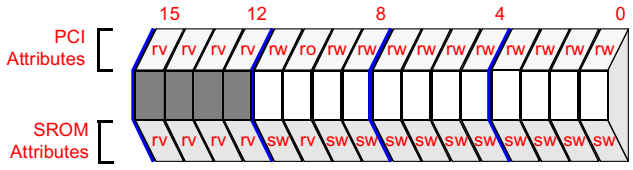
PCI Configuration Address Offset
46h

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:12	0000b	Reserved
11	-b	Opaque Memory Enable: This bit enables the opaque memory base and limit registers. These registers specify a 64 bit memory range that is excluded from the normal decode range of the bridge. A transaction targeting this range on either interface will be ignored by the bridge. 0b = Opaque Memory Range is disabled. 1b = Opaque Memory Range is enabled. **NOTE:** The reset value of this bit is determined by the strapping of the OPAQUE_EN pin.

Table 62. VCR2 - 31154 Bridge Control Register 2 (Sheet 2 of 2)



PCI Configuration Address Offset
46h

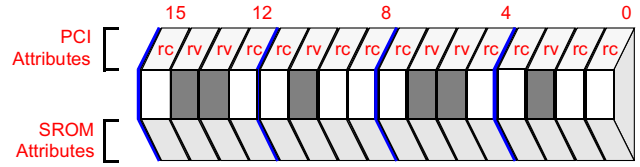
SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
10	-b	Secondary Global Clock Output Enable Status: This bit reflects the status of the S_GCLKOEN input pin. 1b = S_GCLKOEN is high and secondary clock outputs can be enabled. 0b = S_GCLKOEN is low and secondary clock outputs are tri-stated.
09	1b	Secondary Bridge Clock Output Control This bit provides individual enable/disable mask for the S_BRGCLKO output. There is no external strapping option for this bit.
08:00	x xxxx xxxx	Secondary Bus Clock Control: This 9bit field provides individual enable/disable mask bits for each of the secondary PCI clock outputs S_CLKO[8:0]. The reset value is determined by the strapping of S_CLKOEN[3:0] pins. The value on the S_CLKOEN[3:0] pins determines the number of clock outputs (number of bits set) enabled by default. S_CLKOEN[3:0] — Reset Value of bits [08:00] 0000b — 0 0000 0000 0001b — 0 0000 0001 0010b — 0 0000 0011 0011b — 0 0000 0111 0100b — 0 0000 1111 0101b — 0 0001 1111 0110b — 0 0011 1111 0111b — 0 0111 1111 1000b — 0 1111 1111 1001b — 1 1111 1111 . . . . 1111b — 1 1111 1111 0b = Secondary Clock output is tri-stated 1b = Secondary Clock output is enabled **NOTE:** If S_GCLKOEN is pulled low then all clock outputs are tri-stated regardless of the programmed value in this field.

5.2.5 Offset 48H: VSTAT - 31154 Bridge Status

Table 63. VSTAT - 31154 Bridge Status



PCI Configuration Address Offset
48h

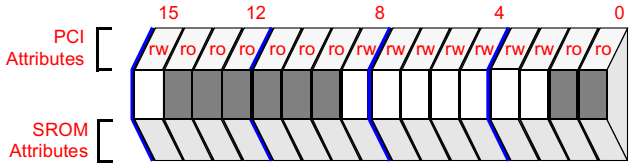
SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15	0b	Upstream Delayed Transaction Discard Timer Expired: This bit is set to a 1b and P_SERR# is conditionally asserted when the secondary discard timer expires.
14	0b	Reserved
13	0b	Reserved
12	0b	Master Abort during Upstream Posted Write: This bit is set to a 1b and P_SERR# is conditionally asserted when a Master Abort occurs as a result of an attempt, by the 31154 Bridge, to retire a PMW upstream.
11	0b	Target Abort during Upstream Posted Write: This bit is set to a 1b and P_SERR# is conditionally asserted when a Target Abort occurs as a result of an attempt, by the 31154 Bridge, to retire a PMW upstream.
10	0b	Reserved
09	0b	Upstream Posted Write Data Parity Error: This bit is set to a 1b and P_SERR# is conditionally asserted when a data parity error is detected by the 31154 Bridge while attempting to retire a PMW upstream.
08	0b	Secondary Bus Address Parity Error: This bit is set to a 1b and P_SERR# is conditionally asserted when the 31154 Bridge detects an address parity error on the secondary bus.
07	0b	Downstream Delayed Transaction Discard Timer Expired: This bit is set to a 1b and P_SERR# is conditionally asserted when the primary bus discard timer expires.
06	0b	Reserved
05	0b	Reserved
04	0b	Master Abort during Downstream Posted Write: This bit is set to a 1b and P_SERR# is conditionally asserted when a Master Abort occurs as a result of an attempt, by the 31154 Bridge, to retire a PMW downstream.
03	0b	Target Abort during Downstream Posted Write: This bit is set to a 1b and P_SERR# is conditionally asserted when a Target Abort occurs as a result of an attempt, by the 31154 Bridge, to retire a PMW downstream.
02	0b	Reserved
01	0b	Downstream Posted Write Data Parity Error: This bit is set to a 1b and P_SERR# is conditionally asserted when a data parity error is detected by the 31154 Bridge while attempting to retire a PMW downstream.
00	0b	Primary Bus Address Parity Error: This bit is set to a 1b and P_SERR# is conditionally asserted when the 31154 Bridge detects an address parity error on the primary bus.

5.2.6 Offset 4AH: SR_ADDR - Serial ROM Address

Table 64. SR_ADDR - Serial ROM Address



PCI Configuration Address Offset
4Ah

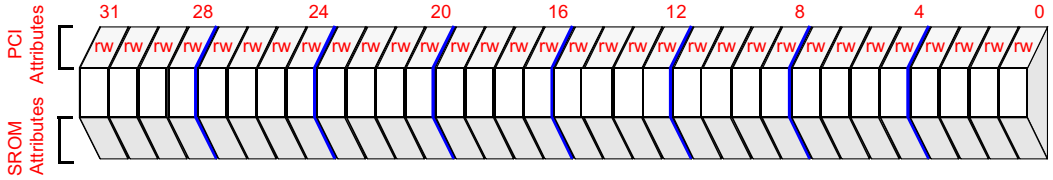
SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15	0b	Serial ROM data direction: 0 = read. 1 = write.
14:09	0h	Reserved
08:02	0000000b	Serial ROM Address Register: This register provides the DWORD address for external serial ROM accesses. Refer to Section 3.4.2.2, “Serial ROM Operation by Configuration Register Access” on page 33 for detailed usage.
01:00	00b	Reserved.

5.2.7 Offset 4CH: SR_DATA - Serial ROM Data

Table 65. SR_DATA - Serial ROM Data



PCI Configuration Address Offset
4Ch

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:00	0000 0000h	Serial ROM Data Register: This register is written with the 32 bits of data to be transferred during serial ROM write operations. When executing a Serial ROM read operation, this register returns the 32-bit read data.

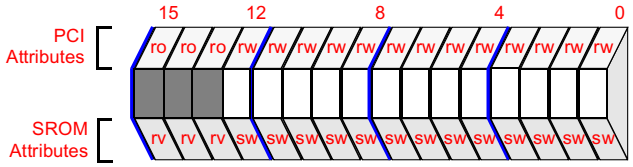
5.2.8 Offset 50H: MTT - Multi-Transaction Timer

The 31154 Bridge Multi-Transaction Timer mechanism (MTT) provides the bridge itself, and any secondary bus master a configurable extended grant duration if desired. The contents of this register have no affect on the operation of the bridge when the internal secondary arbiter is disabled.

The MTT register specifies a common value that establishes a total grant time that applies for all secondary masters. The default value for MTT is 64 PCI clocks.

Refer to Section 4.1, “Arbitration Events” on page 69, and Section 4.2, “Multi-Transaction Timer (MTT)” on page 72 for detailed information regarding the operation of, and rules governing, the Multi-Transaction Timer.

Table 66. MTT - Multi-Transaction Timer



PCI Configuration Address Offset
50h

SROM Offset
08h

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:13	000b	Reserved
12:10	000b	GRANT# Duration: This field specifies the count (in PCI clocks) that a secondary bus master will have its grant maintained in order to enable multiple transactions to execute within the same arbitration cycle. Bit[02:00] GNT# Extended Duration 000MTT Disabled (Default = no GNT# extension) 001 16 clocks 010 32 clocks 011 64 clocks (Default value) 100128 clocks 101256 clocks 110Invalid (treated as 000) 111Invalid (treated as 000)
09:00	3FFh	MTT Mask: This field enables/disables MTT usage for each REQ#/GNT# pair supported by the the 31154 Bridge secondary arbiter. Bit(9) corresponds to the 31154 Bridge internal REQ#/GNT# pair, bit(8) corresponds to REQ#/GNT#(8), etc. When a given bit is set to 1b, its corresponding REQ#/GNT# pair is enabled for MTT functionality as determined by bits(12:10) of this register. When a given bit is cleared to 0b, its corresponding REQ#/GNT# pair is disabled from using the MTT.

5.2.9 Offset 52H: PF_POLICY - Read Prefetch Policy

The Prefetch Policy register is used when the initiating bus is operating in Conventional PCI mode to determine the 31154 Bridge read prefetch parameters.

The amount of data that is to be prefetched is based on the type of read command, i.e., MRL, MRM or a Memory Read targeting pre-fetchable memory space, coupled with the read data demand demonstrated by the PCI initiator.

This register configures a pre-fetchable read byte count based on a "FIRSTREAD" parameter, and a subsequent, larger read byte count based on the "REREAD" parameter that takes affect for a given initiator if its initial demands are not satisfied by the initial pre-fetch amount. (i.e., the 31154 Bridge, not the delayed read transaction initiator, is forced to disconnect the initial read transaction on the originating bus, leaving the initiator waiting for additional read data.)

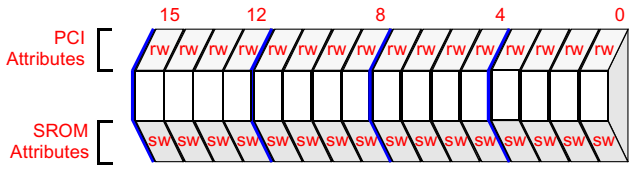
This "smart" pre-fetch policy may be disabled, in which case imposes a fixed pre-fetch policy, also based on read command type. The first three secondary REQ#/GNT# pairs have individual enable/disable bits. A single enable/disable bit governs smart pre-fetch operation for the remainder of the secondary REQ#/GNT# pairs.

The primary bus interface does not require an enable bit. The affect of leaving the Primary bus FirstRead, and ReRead parameters in their power on default states establishes the equivalent behavior.

The 31154 Bridge supports separate smart pre-fetch parameters for the Primary and secondary bus interfaces.

Refer to Section 3.12.5.4, "Prefetching" on page 61 for detailed information regarding the operation of the Prefetch feature.

Table 67. PF_POLICY - Read Prefetch Policy (Sheet 1 of 2)



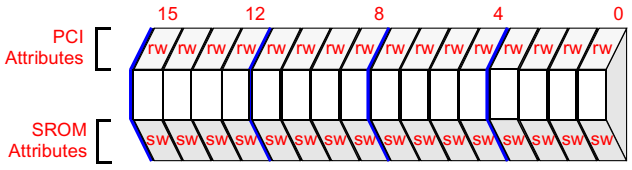
PCI Configuration Address Offset: 52h

SROM Offset: 0Ah

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:13	000b	ReRead_Primary Bus: 3-bit field indicating the multiplication factor to be used in calculating the number of bytes to prefetch from the secondary bus interface on subsequent PreFetch operations given that the read demands were not satisfied using the FirstRead parameter. The default value of 000b correlates to: Command Type — Hardwired pre-fetch amount Mem Read — 4 DWORDs Mem Read Line — 1 cache lines Mem Read Multiple — 2 cache lines

Table 67. PF_POLICY - Read Prefetch Policy (Sheet 2 of 2)



PCI Configuration Address Offset
52h

SROM Offset
0Ah

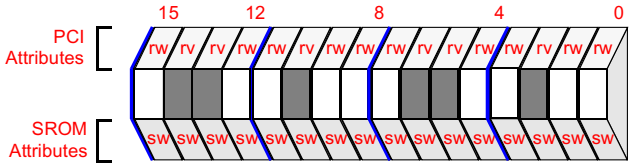
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
12:10	000b	FirstRead_Primary Bus: 3-bit field indicating the multiplication factor to be used in calculating the number of bytes to prefetch from the secondary bus interface on the initial PreFetch operation. The default value of 000b correlates to: Command Type — Hardwired pre-fetch amount Mem Read — 4 DWORDs Mem Read Line — 1 cache line Mem Read Multiple — 2 cache lines
09:07	010b	ReRead_Secondary Bus: 3-bit field indicating the multiplication factor to be used in calculating the number of bytes to prefetch from the primary bus interface on subsequent PreFetch operations given that the read demands were not satisfied using the FirstRead parameter. The default value of 010b correlates to: Command Type — Hardwired pre-fetch amount Mem Read — 3 cache lines Mem Read Line — 3 cache lines Mem Read Multiple — 6 cache lines
06:04	000b	FirstRead_Secondary Bus: 3-bit field indicating the multiplication factor to be used in calculating the number of bytes to prefetch from the primary bus interface on the initial PreFetch operation. The default value of 000b correlates to: Command Type — Hardwired pre-fetch amount Mem Read — 4 DWORDs Mem Read Line — 1 cache line Mem Read Multiple — 2 cache lines
03:00	1111b	Staged Prefetch Enable: This field enables/disables the FirstRead/ReRead pre-fetch algorithm for the secondary and the primary bus interfaces. Bit(3) is a ganged enable bit for REQ#/GNT#[8:3], and bits(2:0) provide individual enable bits for REQ#/GNT#[2:0]. (bit(2) is the enable bit for REQ#/GNT#[2], etc...). 1b: Enables the staged pre-fetch feature. 0b: disables staged pre-fetch, and hardwires read pre-fetch policy to the following for Memory Read, Memory Read Line, and Memory Read Multiple commands: Command Type — Hardwired Pre-Fetch Amount Mem Read — 4 DWORDs Mem Read Line — 1 cache line Mem Read Multiple — 2 cache lines **NOTE:** If the starting address is not cache line aligned, the 31154 Bridge will pre-fetch Mem Read line commands only to the next higher cache line boundary. For non-cache line aligned Mem Read Multiple commands the 31154 Bridge will pre-fetch only to the second cache line boundary encountered.

5.2.10 Offset 54H: SERR_CTL - P_SERR# Assertion Control

This register specifies which events, when detected, cause the 31154 Bridge to assert SERR# on its primary bus. This register does not affect the behavior of the bridge unless the SERR# Enable bit (PCI command register) is set which enables, subject to the further conditions specified herein, the assertion of SERR# on the primary bus.

Table 68. SERR_CTL - P_SERR# Assertion Control (Sheet 1 of 2)



PCI Configuration Address Offset
54h

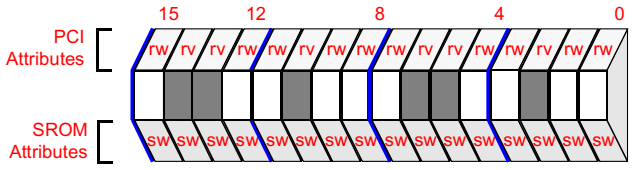
SROM Offset
0Ch

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only

RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15	0b	Upstream Delayed Transaction Discard Timer Expired: Dictates the the 31154 Bridge behavior in response to its discarding of a delayed transaction that was initiated from the primary bus. 0b = the 31154 Bridge asserts P_SERR#. 1b = the 31154 Bridge does not assert P_SERR#.
14	0b	Reserved
13	0b	Reserved
12	0b	Master Abort during Upstream Posted Write: Dictates the 31154 Bridge behavior following its having detected a Master Abort while attempting to retire one of its PMWs upstream. 0b = the 31154 Bridge asserts P_SERR#. 1b = the 31154 Bridge does not assert P_SERR#.
11	0b	Target Abort during Upstream Posted Write: Dictates the 31154 Bridge behavior following its having been terminated with Target Abort while attempting to retire one of its PMWs upstream. 0b = the 31154 Bridge asserts P_SERR#. 1b = the 31154 Bridge does not assert P_SERR#.
10	0b	Reserved
09	0b	Upstream Posted Write Data Parity Error: Dictates the 31154 Bridge behavior when a data parity error is detected while attempting to retire on of its PMWs upstream. 0b = the 31154 Bridge asserts P_SERR#. 1b = the 31154 Bridge does not assert P_SERR#.
08	0b	Secondary Bus Address Parity Error: This bit dictates the 31154 Bridge behavior when it detects an address parity error on the secondary bus. 0b = the 31154 Bridge asserts P_SERR#. 1b = the 31154 Bridge does not assert P_SERR#.
07	0b	Downstream Delayed Transaction Discard Timer Expired: Dictates the 31154 Bridge behavior in response to its discarding of a delayed transaction that was initiated on the secondary bus. 0b = the 31154 Bridge asserts P_SERR#. 1b = the 31154 Bridge does not assert P_SERR#.

Table 68. SERR_CTL - P_SERR# Assertion Control (Sheet 2 of 2)



PCI Configuration Address Offset
54h

SROM Offset
0Ch

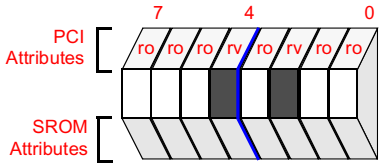
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
06	0b	Reserved
05	0b	Reserved
04	0b	Master Abort during Downstream Posted Write: Dictates the 31154 Bridge behavior following its having detected a Master Abort while attempting to retire one of its PMWs downstream. 0b = the 31154 Bridge asserts P_SERR#. 1b = the 31154 Bridge does not assert P_SERR#.
03	0b	Target Abort during Downstream Posted Write: Dictates the 31154 Bridge behavior following its having been terminated with Target Abort while attempting to retire one of its PMWs downstream. 0b = the 31154 Bridge asserts P_SERR#. 1b = the 31154 Bridge does not assert P_SERR#.
02	0b	Reserved
01	0b	Downstream Posted Write Data Parity Error: Dictates the 31154 Bridge behavior when a data parity error is detected while attempting to retire on of its PMWs downstream. 0b = the 31154 Bridge asserts P_SERR#. 1b = the 31154 Bridge does not assert P_SERR#.
00	0b	Primary Bus Address Parity Error: This bit dictates the 31154 Bridge behavior when it detects an address parity error on the primary bus. 0b = the 31154 Bridge asserts P_SERR#. 1b = the 31154 Bridge does not assert P_SERR#.

5.2.11 Offset 56H: PB_STAT - Pre-Boot Status

This register provides status for each of the strapable and/or serial ROM preloadable configuration settings. Status is updated, and is available immediately following Power On reset.

Table 69. PB_STAT - Pre-Boot Status



PCI Configuration Address Offset
56h

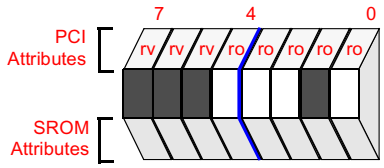
SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07	1b	Secondary 64-Bit Extension Enabled: Indicates whether the secondary bus 64-bit extensions are enabled. 1b = The secondary bus 64-bit extension are enabled. the 31154 Bridge always enables its secondary bus 64-bit extensions.
06	-	Primary 64-Bit Extension Enabled: Indicates whether the primary bus 64-bit extensions are enabled. This is determined by sampling P_REQ64# pin at the rising edge of P_RST#. 0b = The primary bus 64-bit extension is enabled. 1b = The primary bus 64-bit extension is disabled.
05	-	Hot Swap Start up Mode: Indicates the 31154 Bridge behavior when targeted by Type 0 Configuration transactions prior to it's Serial ROM pre-load having completed (i.e., before it is ready to communicate with the host). 0b = the 31154 Bridge retries all Type 0 configuration transactions targeting it. 1b = the 31154 Bridge ignores all Type 0 configuration transactions targeting it thereby causing the transaction to ultimately Master Abort.
04	0b	Reserved
03	-	Internal Arbiter Enable: Indicates whether the secondary internal bus arbiter is enabled. This is determined by sampling ARB_DISABLE during reset. 0b = ARB_DISABLE pin strap was sampled low, causing the secondary bus arbiter to be disabled. 1b = ARB_DISABLE pin strap was sampled high, causing the secondary bus arbiter to be enabled.
02	-	Reserved
01	-	Secondary Bus Max Frequency Setting: This bit reflect the state of the S_MAX100 pin. 0b = The secondary bus in not limited in frequency. 1b = The secondary bus is limited to 100 MHz operation.
00	-	Serial Pre-load Executed: Indicates whether a configuration register pre-load from an external serial ROM had been performed. 0b = The serial pre-load enable sequence was not detected and the register pre-load was not performed. 1b = The serial pre-load enable sequence was detected and the register pre-load was performed.

5.2.12 Offset 57H: MPS - Miscellaneous Pin Status Register

Table 70. MPS - Miscellaneous Pin Status Register



PCI Configuration Address Offset
57h

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:05	000b	Reserved.
04	-b	Secondary Tri-State Status Reflects the current state of the S_TRISTATE pin.
03	-b	New Transaction Mask Status Reflects the state of the NT_MASK#. 0b = New Transaction Mask operation in progress.
02	-b	Arbiter Lock Status Reflects the state of the ARB_DISABLE/ARB_LOCK pin. 0b = Arbiter is locked. Grant is given to the bridge only.
01	-b	Reserved.
00	-b	Hot Swap Latch Status: Reflects the state of the HS_LSTAT pin.

5.2.13 Offset 5CH: Secondary IDSEL Select Register - SISR

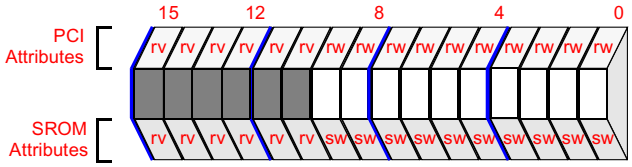
The Secondary IDSEL Select Register controls the usage of **S_AD[25:16]** in Type 1 to Type 0 conversions from the Primary to Secondary interface. In default operation, a unique encoding on Primary addresses **P_AD[15:11]** results in the assertion of one bit on the Secondary address bus **S_AD[31:16]** during a Type 1 to Type 0 conversion. This is used for the assertion of **IDSEL** on the device being targeted by the Type 0 configuration command. This register allows Secondary address bits **S_AD[25:16]** to be used to configure private PCI devices by forcing Secondary address bits **S_AD[25:16]** to all zeros during Type 1 to Type 0 conversions, regardless of the state of Primary addresses **P_AD[15:11]** (device number in Type 1 configuration command).

If any address bit within **S_AD[25:16]** is to be used for private Secondary PCI devices, the user must guarantee that the corresponding bit in the SISR register is set before the host tries to configure the hierarchical PCI buses.

If the IDSEL_MASK pin is sample as 1b on the trailing edge of P_RST# the default value for the this register will be 001Fh to mask devices 0-4.

Note: The "Secondary IDSEL Function 0 Enable Register - SIF0ER" on page 124 **may** be used in conjunction with the SISR. This provides the capability to keep function 0 of a multi-function device public while leaving functions 1-7 private.

Table 71. Secondary IDSEL Select Register - SISR (Sheet 1 of 2)



PCI Configuration Address Offset
5Ch

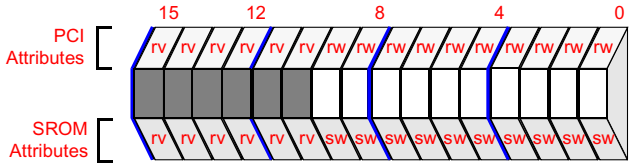
SROM Offset
0Eh

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only

RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:10	000000b	Reserved.
09	0b	**AD25- IDSEL** Disable - When this bit is set, **AD25** will be deasserted for any possible Type 1 to Type 0 conversion. When clear, **AD25** will be asserted when Primary addresses **AD[15:11]** = 01001_2 during a Type 1 to Type 0 conversion.
08	0b	**AD24- IDSEL** Disable - When this bit is set, **AD24** will be deasserted for any possible Type 1 to Type 0 conversion. When clear, **AD24** will be asserted when Primary addresses **AD[15:11]** = 01000_2 during a Type 1 to Type 0 conversion.
07	0b	**AD23 - IDSEL** Disable - When this bit is set, **AD23** will be deasserted for any possible Type 1 to Type 0 conversion. When clear, **AD23** will be asserted when Primary addresses **AD[15:11]** = 00111_2 during a Type 1 to Type 0 conversion.
06	0b	**AD22 - IDSEL** Disable - When this bit is set, **AD22** will be deasserted for any possible Type 1 to Type 0 conversion. When clear, **AD22** will be asserted when Primary addresses **AD[15:11]** = 00110_2 during a Type 1 to Type 0 conversion.
05	0b	**AD21 - IDSEL** Disable - When this bit is set, **AD21** will be deasserted for any possible Type 1 to Type 0 conversion. When clear, **AD21** will be asserted when Primary addresses **AD[15:11]** = 00101_2 during a Type 1 to Type 0 conversion.

Table 71. Secondary IDSEL Select Register - SISR (Sheet 2 of 2)



PCI Configuration Address Offset
5Ch

SROM Offset
0Eh

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
04	-b	**AD20** - **IDSEL** Disable - When this bit is set, **AD20** will be deasserted for any possible Type 1 to Type 0 conversion. When clear, **AD20** will be asserted when Primary addresses **AD[15:11]** = 00100_2 during a Type 1 to Type 0 conversion. The default value will be 1b if the IDSEL_MASK strap is asserted during P_RST#.
03	-b	**AD19** - **IDSEL** Disable - When this bit is set, **AD19** will be deasserted for any possible Type 1 to Type 0 conversion. When clear, **AD19** will be asserted when Primary addresses **AD[15:11]** = 00011_2 during a Type 1 to Type 0 conversion. The default value will be 1b if the IDSEL_MASK strap is asserted during P_RST#.
02	-b	**AD18** - **IDSEL** Disable - When this bit is set, **AD18** will be deasserted for any possible Type 1 to Type 0 conversion. When clear, **AD18** will be asserted when Primary addresses **AD[15:11]** = 00010_2 during a Type 1 to Type 0 conversion. The default value will be 1b if the IDSEL_MASK strap is asserted during P_RST#.
01	-b	**AD17** - **IDSEL** Disable - When this bit is set, **AD17** will be deasserted for any possible Type 1 to Type 0 conversion. When clear, **AD17** will be asserted when Primary addresses **AD[15:11]** = 00001_2 during a Type 1 to Type 0 conversion. The default value will be 1b if the IDSEL_MASK strap is asserted during P_RST#.
00	-b	**AD16** - **IDSEL** Disable - When this bit is set, **AD16** will be deasserted for any possible Type 1 to Type 0 conversion. When clear, **AD16** will be asserted when Primary addresses **AD[15:11]** = 00000_2 during a Type 1 to Type 0 conversion. The default value will be 1b if the IDSEL_MASK strap is asserted during P_RST#.

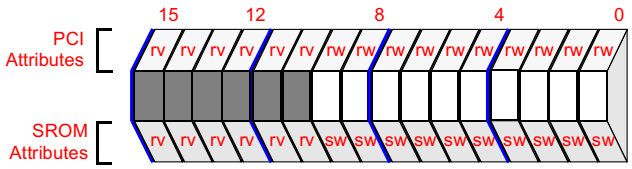
5.2.14 Secondary IDSEL Function 0 Enable Register - SIF0ER

The Secondary IDSEL Function 0 Enable Register together with the Secondary IDSEL Select Register controls the usage of **S_AD[25:16]** in Type 1 to Type 0 conversions from the Primary to Secondary interface. When the SISR register is programmed to allow Secondary address bits **S_AD[25:16]** to be used to configure private PCI devices by forcing Secondary address bits **S_AD[25:16]** to all zeros during Type 1 to Type 0 conversions, the SIF0ER register may be used to reenable the assertion of **IDSEL (S_AD[25:16])** for function 0 (**P_AD[10:8]** must equal 000b) only.

This provides the capability to keep function 0 of a multi-function device public while leaving functions 1-7 private.

Note: The SIF0ER **must** be used in conjunction with the "Offset 5CH: Secondary IDSEL Select Register - SISR" on page 122. Setting of SIF0ER bits is undefined if the corresponding SISR bit is **not** set.

Table 72. Secondary IDSEL Function 0 Enable Register - SIF0ER (Sheet 1 of 2)



PCI Configuration Address Offset
5Eh

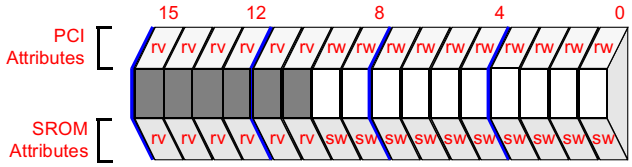
SROM Offset
10h

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only

RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:10	000000_2	Reserved.
09	0_2	**AD25- IDSEL** Function 0 Enable - When this bit is set and SISR bit 9 is set, **AD25** will be asserted when Primary addresses **AD[15:11]** = 01001_2 and Primary addresses **AD[10:8]** = 000_2 during a Type 1 to Type 0 conversion. When this bit is clear and SISR bit 9 is set, **AD25** will be deasserted for any possible Type 1 to Type 0 conversion.
08	0_2	**AD24- IDSEL** Function 0 Enable - When this bit is set and SISR bit 8 is set, **AD24** will be asserted when Primary addresses **AD[15:11]** = 01000_2 and Primary addresses **AD[10:8]** = 000_2 during a Type 1 to Type 0 conversion. When this bit is clear and SISR bit 8 is set, **AD24** will be deasserted for any possible Type 1 to Type 0 conversion.
07	0_2	**AD23- IDSEL** Function 0 Enable - When this bit is set and SISR bit 7 is set, **AD23** will be asserted when Primary addresses **AD[15:11]** = 00111_2 and Primary addresses **AD[10:8]** = 000_2 during a Type 1 to Type 0 conversion. When this bit is clear and SISR bit 7 is set, **AD23** will be deasserted for any possible Type 1 to Type 0 conversion.
06	0_2	**AD22- IDSEL** Function 0 Enable - When this bit is set and SISR bit 6 is set, **AD22** will be asserted when Primary addresses **AD[15:11]** = 00110_2 and Primary addresses **AD[10:8]** = 000_2 during a Type 1 to Type 0 conversion. When this bit is clear and SISR bit 6 is set, **AD22** will be deasserted for any possible Type 1 to Type 0 conversion.
05	0_2	**AD21- IDSEL** Function 0 Enable - When this bit is set and SISR bit 5 is set, **AD21** will be asserted when Primary addresses **AD[15:11]** = 00101_2 and Primary addresses **AD[10:8]** = 000_2 during a Type 1 to Type 0 conversion. When this bit is clear and SISR bit 5 is set, **AD21** will be deasserted for any possible Type 1 to Type 0 conversion.
04	0_2	**AD20- IDSEL** Function 0 Enable - When this bit is set and SISR bit 4 is set, **AD20** will be asserted when Primary addresses **AD[15:11]** = 00100_2 and Primary addresses **AD[10:8]** = 000_2 during a Type 1 to Type 0 conversion. When this bit is clear and SISR bit 4 is set, **AD20** will be deasserted for any possible Type 1 to Type 0 conversion.

Table 72. Secondary IDSEL Function 0 Enable Register - SIF0ER (Sheet 2 of 2)



PCI Configuration Address Offset
5Eh

SROM Offset
10h

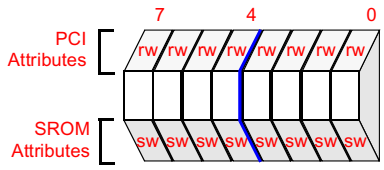
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
03	0_2	**AD19- IDSEL** Function 0 Enable - When this bit is set and SISR bit 3 is set, **AD19** will be asserted when Primary addresses **AD[15:11]** = 00011_2 and Primary addresses **AD[10:8]** = 000_2 during a Type 1 to Type 0 conversion. When this bit is clear and SISR bit 3 is set, **AD19** will be deasserted for any possible Type 1 to Type 0 conversion.
02	0_2	**AD18- IDSEL** Function 0 Enable - When this bit is set and SISR bit 2 is set, **AD18** will be asserted when Primary addresses **AD[15:11]** = 00010_2 and Primary addresses **AD[10:8]** = 000_2 during a Type 1 to Type 0 conversion. When this bit is clear and SISR bit 2 is set, **AD18** will be deasserted for any possible Type 1 to Type 0 conversion.
01	0_2	**AD17- IDSEL** Function 0 Enable - When this bit is set and SISR bit 1 is set, **AD17** will be asserted when Primary addresses **AD[15:11]** = 00001_2 and Primary addresses **AD[10:8]** = 000_2 during a Type 1 to Type 0 conversion. When this bit is clear and SISR bit 1 is set, **AD17** will be deasserted for any possible Type 1 to Type 0 conversion.
00	0_2	**AD16- IDSEL** Function 0 Enable - When this bit is set and SISR bit 0 is set, **AD16** will be asserted when Primary addresses **AD[15:11]** = 00000_2 and Primary addresses **AD[10:8]** = 000_2 during a Type 1 to Type 0 conversion. When this bit is clear and SISR bit 0 is set, **AD16** will be deasserted for any possible Type 1 to Type 0 conversion.

5.2.15 Offset 68H: GPIO_PINCFG - GPIO Pin Configuration Register

This register configures each of the GPIO pins as either an input only or as a R/W output. Bit(0) corresponds to GPIO(0), Bit(1) corresponds to GPIO(1), and so on.

Table 73. GPIO_PINCFG - GPIO Pin Configuration Register



PCI Configuration Address Offset
68h

SROM Offset
12h

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

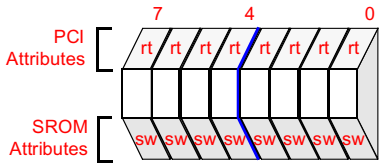
Bit	Default	Description
07:00	00h	GPIO Pin Configuration: Writing 1b to any of these bits configures their corresponding GPIO pin as an output. The default value of this register is 00h, configuring all of the GPIO pins as inputs.

5.2.16 Offset 69H: GPIO_W1TT_DATA - Output Data “Write One to Toggle” Register

Software writes to this read/write register to toggle one or more GP output states. Reads of this register return the current logical state of the GPIOs, had they been configured as outputs.

Writing 0b to any bit or bits in this register has no affect.

Table 74. GPIO_W1TT_DATA - Output Data “Write One to Toggle” Register



PCI Configuration Address Offset
69h

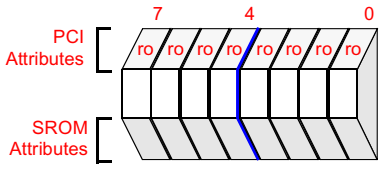
SROM Offset
13h

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	00b	GPO Write 1b to Toggle: Writing 1b to any of these bits causes their corresponding GPO state to toggle. This register may be read by software at any time. The value returned when reading this register corresponds to the current logic output levels for each of the GPIOs had they been configured as outputs; not to be confused with the actual state of the GPIO pins. The actual state of the GPIO pins can be observed by reading the Pin Status register. (described in the next section).

5.2.17 Offset 6AH: GPIO_PINSTAT - GPIO Pin Status Register

Table 75. GPIO_PINSTAT - GPIO Pin Status Register



PCI Configuration Address Offset
6Ah

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

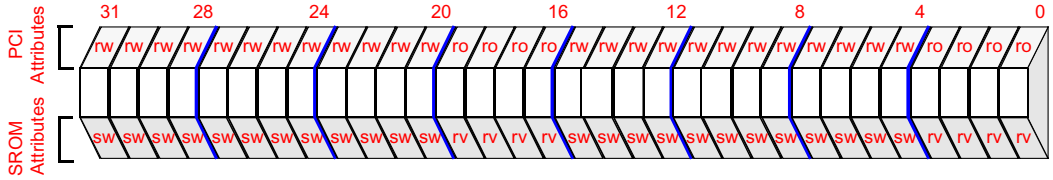
Bit	Default	Description
07:00	-	GPIO Pin Status: Reading this register returns the current state of the GPIO pins.

5.2.18 Offset 6CH: OMBL - Opaque Memory Base and Limit Register

This register defines, by way of base and limit fields, an opaque memory mapped I/O address range. Memory transactions originating on either the primary or secondary bus that address a memory location falling within the opaque range are ignored bye the bridge and not passed in either direction.

The Opaque Memory Enable bit in the "VCR2 - 31154 Bridge Control Register 2" on page 110 must be set to enable the Opaque memory window. The default values configure the upper half of memory (P_AD[63] = 1) as an opaque region.

Table 76. OMBL - Opaque Memory Base and Limit Register



PCI Configuration Address Offset
6Ch

SROM Offset
15h

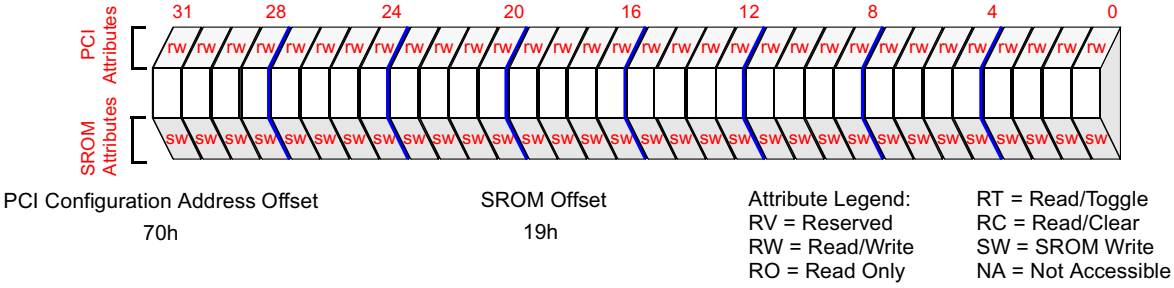
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:20	FFFh	Opaque Memory Limit: These 12 bits are compared with P_AD[31:20] of the incoming address to determine the upper 1MB aligned value (exclusive) of the range. The incoming address must be less than or equal to this value. For the purposes of address decoding the lower 20 address bits (P_AD[19:0]) are assumed to be F FFFFh.
19:16	1h	64-bit Indicator: Indicates that 64-bit addressing is supported.
15:04	000h	Opaque Memory Base: These 12 bits are compared with bits P_AD[31:20] of the incoming address to determine the lower 1MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value. For the purposes of address decoding the lower 20 address bits (P_AD[19:0]) are assumed to be 0 0000h.
03:00	1h	64-bit Indicator: Indicates that 64-bit addressing is supported.

5.2.19 Offset 70H: OMBU32 - Opaque Memory Base Upper 32 Bits

This defines the upper 32 bits of the opaque address base register.

Table 77. OMBU32 - Opaque Memory Base Upper 32 Bits



PCI Configuration Address Offset
70h

SROM Offset
19h

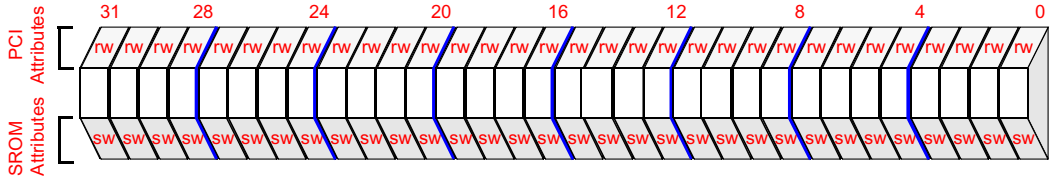
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:00	8000 0000h	Opaque Memory Base Upper Portion: All bits are read/writeable - the 31154 Bridge supports full 64-bit addressing.

5.2.20 Offset 74H: OMLU32 - Opaque Memory Limit Upper 32 Bits

This defines the upper 32 bits of the opaque address base register.

Table 78. OMBU32 - Opaque Memory Limit Upper 32 Bits



PCI Configuration Address Offset
74h

SROM Offset
1Dh

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:00	FFFF FFFFh	Opaque Memory Base Upper Portion: All bits are read/writeable - the 31154 Bridge supports full 64-bit addressing.

5.3 PCI Extended Capabilities List

The following sections detail the programming interface for the 31154 Bridge Capabilities List. This standard link list infrastructure lays out the programming model for the following extended capabilities:

- *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a compliant.
- *PCI Bus Power Management Interface Specification*, Revision 1.1 compliant.
- *Compact PCI Hot Swap Specification*, Revision 2.1 R2.0 compliant.
- PCI Chassis/Slot Identification.
- Vital Product Data (VPD).

Table 79 outlines the address map for the extended capabilities, followed by the individual sub sections where full interface details are provided.

Table 79. Enhanced Capabilities Register File

Byte 3	Byte 2	Byte 1	Byte 0	Configuration Byte Offset
Chassis Number$^{\Psi}$	Slot Number$^{\Psi}$	Next Item Ptr	Capability ID	D4h
Reserved				D8h
Power Management Capabilities$^{\Psi}$		Next Item Ptr$^{\Psi}$	Capability ID	DCh
PM Data	PPB Support Extensions	Power Management CSR		E0h
VPD Address		Next Item Ptr	Capability ID	E4h
VPD Data				E8h
Reserved	Hot Swap Control	Next Item Ptr	Capability ID	ECh
PCI-X Secondary Status		Next Item Ptr$^{\Psi}$	Capability ID	F0h
PCI-X Bridge Status				F4h
PCI-X Upstream Split Transaction Control				F8h
PCI-X Downstream Split Transaction Control				FCh

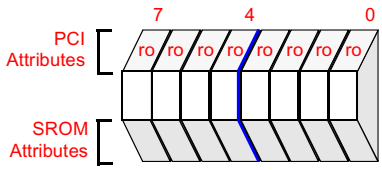
NOTE: $^{\Psi}$ Register values may be pre-loaded using the serial ROM interface.

5.3.1 PCI Chassis and Slot Identification

The following sections provide PCI and Slot Identification for the 31154 Bridge.

5.3.1.1 Offset D4h: CS_CID - Chassis/Slot Capability ID

Table 80. CS_CID - Chassis/Slot Capability ID



PCI Configuration Address Offset: D4

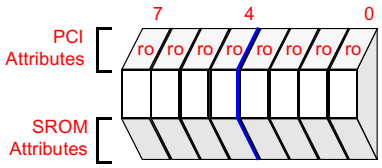
SROM Offset: NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	04h	Cap ID for Chassis and Slot capability.

5.3.1.2 Offset D5h: CS_NXTP - Next Item Pointer

Table 81. CS_NXTP - Next Item Pointer



PCI Configuration Address Offset
D5h

SROM Offset
NA

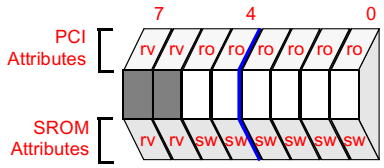
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	DCh	Next Capabilities Pointer (PTR) (PCI-PM Registers).

5.3.1.3 Offset D6h: SLT_NUM - Slot Number

This register is pre-loadable from the Serial ROM.

Table 82. SLT_NUM - Slot Number



PCI Configuration Address Offset
D6h

SROM Offset
21h

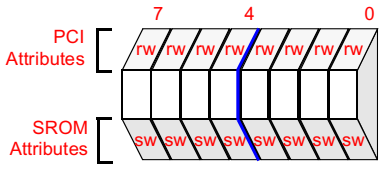
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:06	00b	Reserved
05	0	First in Chassis: If this bit is set, it indicates that this bridge is the first in an expansion chassis. A bridge with this set indicates the existence of an expansion chassis that requires a unique chassis number. The default value is preloadable via SROM.
04:00	00h	Expansion Slots Provided: Contains the binary value of the number of PCI expansion slots located directly on the secondary interface of this bridge. Expansion slots located behind additional (subordinate) bridges on the secondary interface are not counted in the this field. The default value is preloadable via SROM.

5.3.1.4 Offset D7h: CS_NUM - Chassis Number

This register is pre-loadable from the Serial ROM.

Table 83. CS_NUM - Chassis Number



PCI Configuration Address Offset
D7h

SROM Offset
22h

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

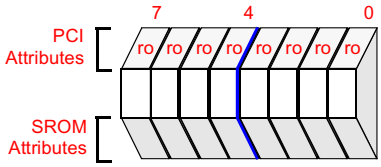
Bit	Default	Description
07:00	00h	Chassis Number. The default value is preloadable via SROM.

5.3.2 PCI Bus Power Management

5.3.2.1 Offset DCh: PM_CAPID - Power Management Capabilities Identifier

Read by system software as 01h to indicate that this is the PCI Power Management data structure.

Table 84. PM_CAPID - Power Management Capabilities Identifier



PCI Configuration Address Offset
DCh

SROM Offset
NA

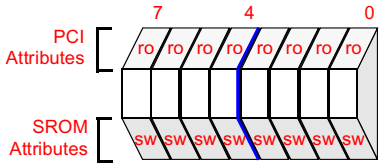
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	01h	Identifier (ID): PCI SIG assigned ID for PCI-PM register block.

5.3.2.2 Offset DDh: PM_NXTP - Next Item Pointer

This points to the next item in the function's capability list. If VPD functionality is desired then this register must be pre-loaded by the Serial ROM with E4h to expose the VPD register block.

Table 85. PM_NXTP - Next Item Pointer



PCI Configuration Address Offset
DDh

SROM Offset
23h

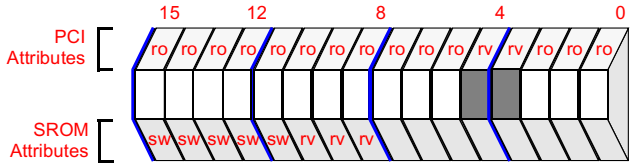
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	ECh; Serial ROM Pre-loadable to E4h to expose VPD register i/f	Next Capabilities Pointer (PTR): The register defaults to ECh essentially skipping over the VPD register block and pointing instead to the cPCI Hot Swap registers. In order to make the VPD register block visible to software the optional Serial ROM must be deployed, and it must pre-load this register with a value of E4h. If E4h is pre-loaded by the Serial ROM then the VPD registers are pointed to here. In this case the VPD Next Item register in turn points to the cPCI How Swap register i/f.

5.3.2.3 Offset DEh: PM_C - Power Management Capabilities

This register reports the 31154 Bridge power management capabilities. This register can be Serial ROM pre-loaded, enabling the PME Support bits (15:11) to be set to all ones circumventing a Win98 PM errata with bridges.

Table 86. PM_C - Power Management Capabilities



PCI Configuration Address Offset: DEh

SROM Offset: 24h

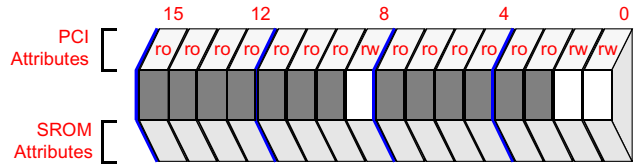
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:11	00h	PME Supported (PME): PME# cannot be asserted by the 31154 Bridge. However to work around a PM bug in some versions of Win98 these bits can be serial ROM pre-loaded with all 1s.
10	0h	State D2 Supported (D2): Indicates no support for state D2. No power management action in this state.
09	1h	State D1 Supported (D1): Indicates support for state D1. No power management action in this state.
08:06	0h	Auxiliary Current (AUXC): This 3 bit field reports the 3.3Vaux auxiliary current requirements for the PCI function. This returns 000b as PME# wake-up for the 31154 Bridge is not implemented.
05	0	Special Initialization Required (SINT): Special initialization is not required for the 31154 Bridge.
04:03	00	Reserved.
02:00	010	Version (VS): Indicates that this supports *PCI Bus Power Management Interface Specification*, Revision 1.1.

5.3.2.4 Offset E0h: PM_CS - Power Management Control / Status

This register is used to manage the 31154 Bridge power management state as well as to enable/ monitor PMEs.

Table 87. PM_CS - Power Management Control / Status



PCI Configuration Address Offset
E0h

SROM Offset
NA

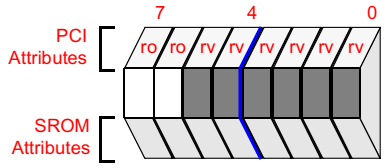
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:09	00h	Reserved.
08	0b	PME_Enable: This bit, when set to 1b enables the 31154 Bridge to assert PME#. Note that the 31154 Bridge never has occasion to assert PME# and implements this dummy R/W bit only for the purpose of working around an OS PCI-PM bug.
07:02	00h	Reserved.
01:00	00	Power State (PSTATE): This 2-bit field is used both to determine the current power state of a function and to set the Function into a new power state. 00 - D0 state 01 - D1 state 10 - D2 state 11 - $D3_{hot}$ state

5.3.2.5 Offset E2h: PM_CS_BSE - Power Management Control / Status PCI to PCI Bridge Support

Indicates support for PCI bridge specific functionality.

Table 88. PM_CS_BSE - Power Management Control / Status PCI to PCI Bridge Support



PCI Configuration Address Offset: E2h

SROM Offset: NA

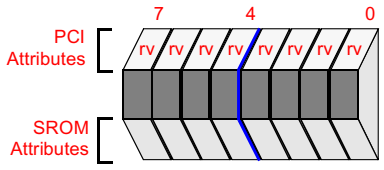
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07	0	Bus Power/Clock Control Enable (BPCC_En): Indicates that the bus power/clock control policies have been disabled.
06	0	B2/B3 support for D3 Hot (B2_B3#): The state of this bit determines the action that is to occur as a direct result of programming the function to D3 hot. This bit is only meaningful if bit 7 (BPCC_En) is a “1”.
05:00	00h	Reserved.

5.3.2.6 Offset E3h: PM_DATA - Power Management Data

The data register is not supported.

Table 89. PM_DATA - Power Management Data



PCI Configuration Address Offset
E3h

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

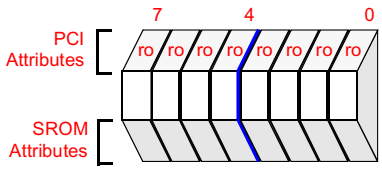
Bit	Default	Description
07:00	00h	Reserved.

5.3.3 Vital Products Data (VPD)

5.3.3.1 Offset E4h: VPD_CAPID - VPD Capabilities Identifier

Read by system software as 03h indicating that the data structure currently being pointed to is the VPD data structure.

Table 90. VPD_CAPID - VPD Capabilities Identifier



PCI Configuration Address Offset
E4h

SROM Offset
NA

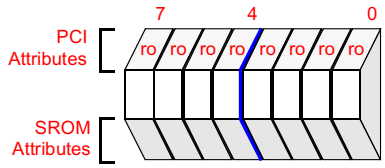
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	03h	Identifier (ID): As 03h, identifies linked list item as being Vital Product Data (VPD) registers.

5.3.3.2 Offset E5h: VPD_NXTP - Next Item Pointer

This describes the location of the next item in the function's capability list.

Table 91. VPD_NXTP - Next Item Pointer



PCI Configuration Address Offset
E5h

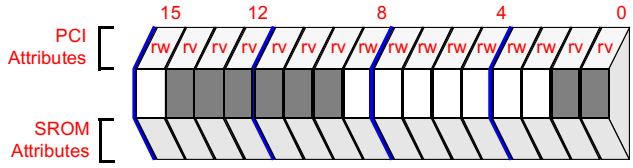
SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	ECh	Next Capabilities Pointer (PTR): Indicates offset ECh contains next capabilities pointer (Hot Swap registers).

5.3.3.3 Offset E6h: VPD_ADDR - VPD Address Register

Table 92. VPD_ADDR - VPD Address Register



PCI Configuration Address Offset
E6h

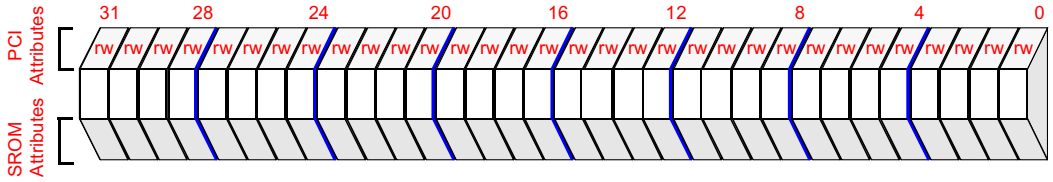
SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15	0b	VPD Flag: Starts a VPD Serial ROM access and indicates completion of operation. When written to 0b: A 4-byte serial ROM read is performed starting at the VPD DWORD aligned location indicated by bits [8:2]. When the read is complete, the 31154 Bridge sets this bit to 1b. When written to 1b: A 4-byte serial ROM write is performed starting at the VPD DWORD aligned location indicated by bits [8:2]. When the write is complete, the 31154 Bridge clears this bit to 0b.
14:09	000000b	Reserved
08:02	0000000b	VPD Address: Contains the VPD DWORD address of the serial ROM location to be accessed. Valid VPD byte addresses are 17C: 000h. VPD starts at base address 080h in the serial ROM. The VPD DWORD aligned address contained in this register is added to the VPD base address to obtain the final serial ROM address.
01:00	00b	Reserved.

5.3.3.4 Offset E8h: VPD_DATA - VPD Data Register

Table 93. VPD_DATA - VPD Data Register



PCI Configuration Address Offset
E8h

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

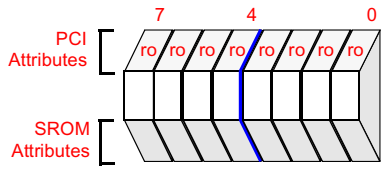
Bit	Default	Description
31:00	00000000h	VPD Data: Contains VPD read or write data. For a read, this register should be read after a read operation was initiated and the 31154 Bridge has returned the VPD Flag bit to a 1b. For a write, this register should be written with the write data before operation is initiated with a write to the VPD Address and VPD Flag bits. VPD read and write operations are always 4-byte operations. Byte 0, (bits(7:0)), represents the least significant byte.

5.3.4 CompactPCI* Hot Swap

The following register block provides support of CompactPCI* Hot Swap functionality.

5.3.4.1 Offset ECh: HS_CAPID - Hot Swap Cap ID

Table 94. HS_CAPID - Hot Swap Cap ID



PCI Configuration Address Offset: ECh

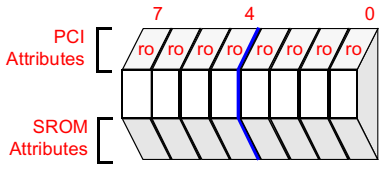
SROM Offset: NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	06h	Identifier (ID): 06h, identifying this linked list structure as being the Compact PCI Hot Swap register block.

5.3.4.2 Offset EDh: HS_NXTP - Next Item Pointer

Table 95. HS_NXTP - Next Item Pointer



PCI Configuration Address Offset: EDh

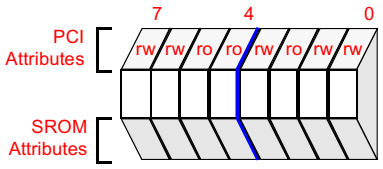
SROM Offset: NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	F0h	Next Capabilities Pointer (PTR): Points to next capability in the linked list of capabilities (PCI-X registers).

5.3.4.3 Offset EEh: HS_CNTRL - Hot Swap Control/Status Register

Table 96. HS_CNTRL - Hot Swap Control/Status Register (Sheet 1 of 2)



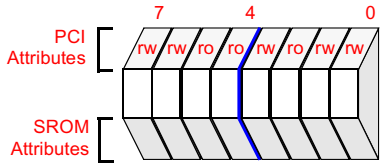
PCI Configuration Address Offset: EEh

SROM Offset: NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07	1b (This bit actually powers up to 0b, however the 31154 Bridge will set it to 1b prior to any host software access to the device)	INS: Freshly INSerted board. the 31154 Bridge sets this bit to a 1b following the de-assertion of P_RST# provided that: • L_STAT is sampled low indicating that the ejector handle closed. • The Serial ROM pre-load has completed (if one was executed). The INS bit is cleared when software writes a 1b to it. Writing 0b to this bit has no effect. 1b = the 31154 Bridge asserts P_ENUM#, (if not masked by bit(1) of this register), to indicate that the card is freshly inserted and is ready to be configured by system software. After system software has cleared this bit (by writing a 1b to it) the 31154 Bridge de-asserts P_ENUM# (if currently asserted), and is then armed for a possible future extraction event (EXT bit assertion is enabled).
06	0b	EXT: Pending EXTraction of board. the 31154 Bridge sets this bit to a 1b when: • L_STAT is sampled high while P_RST# is deasserted indicating that the ejector handle is unlocked. • The board is currently in the INSERTED state (i.e., the INS bit = 0b). The EXT bit is cleared when software writes a 1b. Writing a 0b has no effect.When 1b: the 31154 Bridge asserts P_ENUM#, (if not masked by bit(1) of this register), to indicate that the card is about to be removed.
05:04	01b	PI: Programming Interface This field is hard-wired to 01b indicating that the 31154 Bridge supports Device Hiding and PIE bit functionality.
03	0b	LOO: LED On/Off (LOO) Control. Allows software control of the LED. When 0b: the 31154 Bridge will drive LED_OUT low turning the external LED off. When 1b: the 31154 Bridge will drive LED_OUT high illuminating the external LED. **NOTE:** Additional external LED control logic must be ORd with the 31154 Bridge LED_OUT signal to ensure that the blue LED is illuminated while P_RST# is asserted or when the board is in the H0, H1, or H1F cPCI Hot Swap defined hardware states.

Table 96. HS_CNTRL - Hot Swap Control/Status Register (Sheet 2 of 2)



PCI Configuration Address Offset
EEh

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

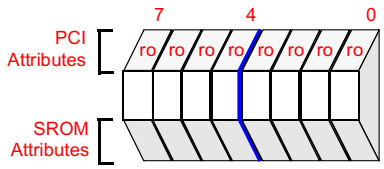
Bit	Default	Description
02	0b	PIE: Pending Insertion/Extraction This status bit is set and cleared by the the 31154 Bridge Hot Swap state Machine. When 1b this bit indicates that either an insertion or an extraction is in progress (either INS or EXT has a value of 1b or INS is armed).
01	0b	EIM: ENUM# Interrupt Mask. When 0b: the 31154 Bridge asserts P_ENUM# when an insertion or removal event occurs as indicated by the setting of the INS or EXT bits of this register. When 1b: the 31154 Bridge will not assert P_ENUM# under any circumstances.
00	0b	DHA: Device Hiding Armed: When 1b: If HS_SM = 1b, and LSTAT = 1b (Switch open) and the LOO bit = 1b, the 31154 Bridge will complete any bus cycles presently in process and then cease to initiate or respond to either primary or secondary bus cycles. If LSTAT subsequently goes low, the 31154 Bridge will respond normally to bus cycles. When 0: the 31154 Bridge operates normally.

5.3.5 *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a

5.3.5.1 Offset F0h: PX_CAPID - PCI-X Capabilities Identifier

Identifies this item in the Capabilities list as a PCI-X register set. It returns 07h when read.

Table 97. PX_CAPID - PCI-X Capabilities Identifier



PCI Configuration Address Offset: F0h

SROM Offset: NA

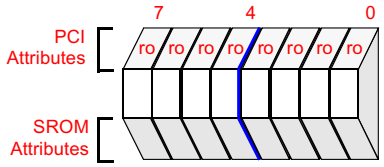
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	07h	Identifier (ID): Indicates this is a PCI-X capabilities list.

5.3.5.2 Offset F1h: PX_NXTP - Next Item Pointer

Indicates where the next item in the capabilities list resides. The PCI-X capability register block is the end of the the 31154 Bridge Capabilities List, so “00h” is the power on reset default state.

Table 98. PX_NXTP - Next Item Pointer



PCI Configuration Address Offset
F1h

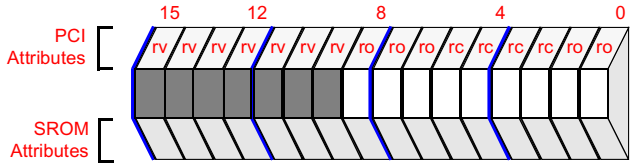
SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
07:00	00h	Next Item Pointer: Points to the next capability in the linked list The power on default value of this register is 00h indicating that this is the last entry in the linked list of capabilities.

5.3.5.3 Offset F2h: PX_SSTS - PCI-X Secondary Status

Table 99. PX_SSTS - PCI-X Secondary Status



PCI Configuration Address Offset
F2h

SROM Offset
NA

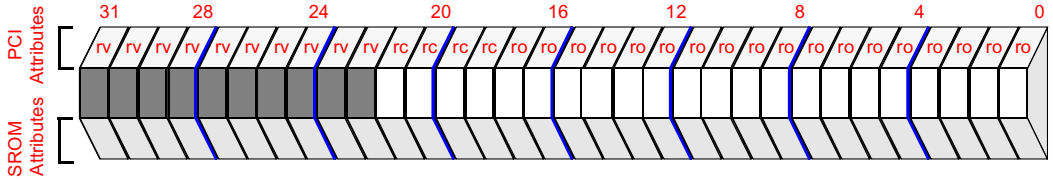
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
15:09	00h	Reserved
08:06	0xx	Secondary Clock Frequency (SCF): This field is set with the frequency of the secondary bus. The values are: Bits / Max Frequency / Clock Period 000 / PCI Mode / N/A 001 / 66 / 15 010 / 100 / 10 011 / 133 / 7.5 1xx / reserved / reserved The default value for this register is the operating frequency of the secondary bus.
05	0b	Split Request Delayed. (SRD): This bit is set by the bridge if it cannot forward a transaction on the secondary bus because there is not enough room within the limit specified in the Split Transaction Commitment Limit field in the Downstream Split Transaction Control register. the 31154 Bridge does not implement this feature and will never set this bit.
04	0b	Split Completion Overrun (SCO): This bit is set if the bridge terminates a Split Completion on the secondary bus with Retry or Disconnect at next ADB because its buffers are full. the 31154 Bridge does not implement this feature and will never set this bit.
03	0b	Unexpected Split Completion (USC): This bit is set if an unexpected split completion with a requester ID equal to the the 31154 Bridge secondary bus number, device number 00h, and function number 0 is received on the secondary interface. This bit is cleared by software writing a '1'.
02	0b	Split Completion Discarded (SCD): This bit is set if the 31154 Bridge discards a split completion moving toward the secondary bus because the requester would not accept it. This bit cleared by software writing a '1'.
01	1b	133 MHz Capable: Indicates that the 31154 Bridge is capable of running its secondary bus at 133 MHz.
00	1b	64-bit Device (D64): Indicates the width of the secondary bus as 64-bits.

5.3.5.4 Offset F4h: PX_BSTS - PCI-X Bridge Status

Identifies PCI-X capabilities and current operating mode of the bridge.

Table 100. PX_BSTS - PCI-X Bridge Status



PCI Configuration Address Offset
F4h

SROM Offset
NA

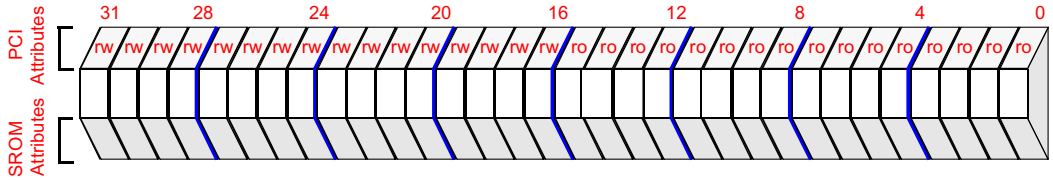
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:22	0	Reserved
21	0	Split Request Delayed (SRD): This bit is set any time the bridge has a request to forward a transaction on the primary bus but cannot because there is not enough room within the limit specified in the Split Transaction Commitment Limit field in the Upstream Split Transaction Control register. the 31154 Bridge does not implement this feature and will never set this bit.
20	0	Split Completion Overrun (SCO): This bit is set if the bridge terminates a Split Completion on the primary bus with a Retry or Disconnect at the Next ADB because the bridge buffers are full. the 31154 Bridge does not implement this feature and will never set this bit.
19	0	Unexpected Split Completion (USC): This bit is set to 1b if the bridge encounters a corrupted Split Completion, possibly with an inconsistent remaining byte count.Software clears this bit by writing a 1b to it.
18	0	Split Completion Discarded (SCD): This bit is set to 1b if the bridge discarded a Split Completion. Software clears this bit by writing 1b to it.
17	1	133 MHz Capable: This bit indicates that the bridge primary interface is capable of 133 MHz operation in PCI-X mode. 0 = The maximum operating frequency is 66 MHz. 1 = The maximum operating frequency is 133 MHz.
16	-	64-bit Device (D64): This bit is set by the DEV_64BIT# strap. It is electrically the inverse of the strap, so pulling DEV_64BIT# low will set this bit to 1b. 1b = Indicates the 31154 Bridge is a 64 bit device.
15:08	00h	Bus Number (BNUM): This field is simply an alias to the PBN field of the BNUM register at offset 18h. Apparently it was deemed necessary reflect it here for diagnostic purposes.
07:03	1Fh	Device Number (DNUM): Indicates which IDSEL the 31154 Bridge consumes. May be updated whenever a PCI-X configuration write cycle that targets the 31154 Bridge scores a hit.
02:00	0h	Function Number (FNUM): The bridge is function 0.

5.3.5.5 Offset F8h: PX_USTC - PCI-X Upstream Split Transaction Control

This register identifies controls behavior of the the 31154 Bridge buffers for forwarding Split Transactions from the secondary bus to primary.

Table 101. PX_USTC - PCI-X Upstream Split Transaction Control



PCI Configuration Address Offset: F8h

SROM Offset: NA

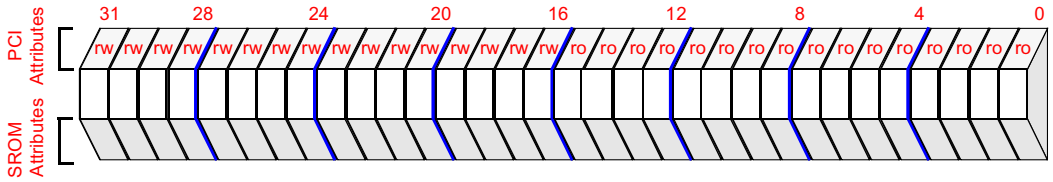
Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:16	003Eh	Split Transaction Limit (STL): This register indicates the size of the commitment limit in units of ADQs. Software is permitted to program this register to any value greater than or equal to the contents of the Split Transaction Capacity register. A value less than the contents of the Split Transaction Capacity register causes unspecified results. A value of 003Eh or greater will enable the bridge to forward all Split Requests of any size regardless of the amount of buffer space available.
15:00	003Eh	Split Transaction Capacity (STC): This read-only field indicates the size of the buffer (in number of ADQs) for storing split completions. This register controls behavior of the bridge buffers for forwarding Split Transactions from a primary bus requester to a secondary bus completer. The default value of 003Eh indicates there is available buffer space for 62 ADQs (7936 bytes).

5.3.5.6 Offset FCh: PX_DSTC - PCI-X Downstream Split Transaction Control

This register controls behavior of the 31154 Bridge buffers for forwarding Split Transactions from primary to the secondary bus.

Table 102. PX_DSTC - PCI-X Downstream Split Transaction Control



PCI Configuration Address Offset
FCh

SROM Offset
NA

Attribute Legend:
RV = Reserved
RW = Read/Write
RO = Read Only
RT = Read/Toggle
RC = Read/Clear
SW = SROM Write
NA = Not Accessible

Bit	Default	Description
31:16	003Eh	Split Transaction Limit (STL): This register indicates the size of the commitment limit in units of ADQs. Software is permitted to program this register to any value greater than or equal to the contents of the Split Transaction Capacity register. A value less than the contents of the Split Transaction Capacity register causes unspecified results. A value of 003Eh or greater will enable the bridge to forward all Split Requests of any size regardless of the amount of buffer space available.
15:00	003Eh	Split Transaction Capacity (STC): This read-only field indicates the size of the buffer (in number of ADQs) for storing split completions. This register controls behavior of the bridge buffers for forwarding Split Transactions from a secondary bus requester to a primary bus completer. The default value of 003Eh indicates there is available buffer space for 62 ADQs (7936 bytes).

Error Detection and Reporting 6

Error detection and reporting are separate items within the 31154 Bridge. Error detection is a continuous on going operation. Every detected error is logged in the status bits for reporting errors at all times.

When error reporting is enabled for an interface; PER set in the Command and Bridge Control registers for the primary and secondary busses respectively allows the 31154 Bridge to respond to error detection. Further, errors can be reported to the system by the assertion of P_SERR#, which is enable by the SERR# Enable bit in the Command register.

During normal operation all transactions are passed from one interface to the other without modification, unless they require special action by the 31154 Bridge. All phases of a transaction are passed from one bus to the other without modification including address and attributes.

6.1 Normal Operation

Address, attributes and data are accepted on the Origination Bus and passed without modification for most types of transactions. Parity for each phase of a transaction is also passed though the bridge without modification. Parity is generated by the 31154 Bridge for the following types of transactions:

- Type 1 configuration to Special cycle conversion.
- Type 1 configuration to Type 0 conversion.
- 31154 Bridge generated Split Completions.

Detection of errors always results in the error detection state being set. This is true for all types of errors detected by the 31154 Bridge.

6.2 Response Enabled

Each bus has a separate PER control bit to enable the 31154 Bridge responding to errors. When the PER bit is set the 31154 Bridge takes action on each transaction depending on the type of error. Types of errors on which action is taken are:

Table 103. Detected Error Types and Action Taken

Error Type	Action Taken
address or attribute parity	For all transactions in error it sets the Detected Parity Error bit in the associated buses Status register. Conditionally sets Signaled System Error bit in the Status register when it causes an assertion of SERR#.
	Split Completion: Target Abort transactions and discard associated data. Note: If an Attribute Parity error occurs for a single data phase transcation, the bridge will forward the data to the other interface with bad attribute parity.
	Other transaction: Generates a SCM response to all transactions needing a Split Completion response. Discard transaction and associated data.
data parity	Sets Detected Parity Error bit in the Status register. Asserts x_PERR# on the associated bus.
	PCI-X transaction: Store and forward all data including parity bit.
	Delayed transaction: Discard transaction and purge data from buffers.
x_PERR# assertion by external agent	Set Master Data Parity Error bit in the Status register for the associated bus.
Master Abort	Set Received Master Abort bit in the associated Status register. Conditionally sets Signaled System Error bit in the Status register when it causes an assertion of SERR#.
	PCI and read: Send FFFFFFFFh as read data on the Origination bus.
	PCI-X: Generate a SCM message to all transactions that received a split response.
Target Abort	Set Received Target Abort bit in the associated Status register.
	Posted Memory Write: Conditionally sets Signaled System Error bit in the Status register when it causes an assertion of SERR#.
S_SERR#	Set the Received System Error bit in the Secondary Status Register. Conditionally sets Signaled System Error bit in the Status register when it causes an assertion of P_SERR#.
Discard Timer	Set the Discard Timer bit in the associated Status register. Conditionally sets Signaled System Error bit in the Status register when it causes an assertion of SERR#.
Retry Timer	After 2^{24} retries on the destination bus discard the transaction. Conditionally sets Signaled System Error bit in the Status register when it causes an assertion of SERR#.
Unexpected Split Completion	When a Split Completion does not match byte count, or address field is incorrect. Conditionally sets Signaled System Error bit in the Status register when it causes an assertion of SERR#.

6.3 P_SERR# Assertion

Asserted when an error capable of SERR# assertion occurs, the SERR# enable bit in the Command register is set, and that particular error condition has been enabled to assert P_SERR# in the P_ERR# Assertion Control Register. In all cases the assertion of SERR# results in setting of the Signaled System Error bit in the Status register.

Testability 7

7.1 JTAG Overview

Boundary Scan is a standard DFT architecture that is incorporated at the IC level, used in both device level, board level, and system level testing. The JTAG architecture is composed of:

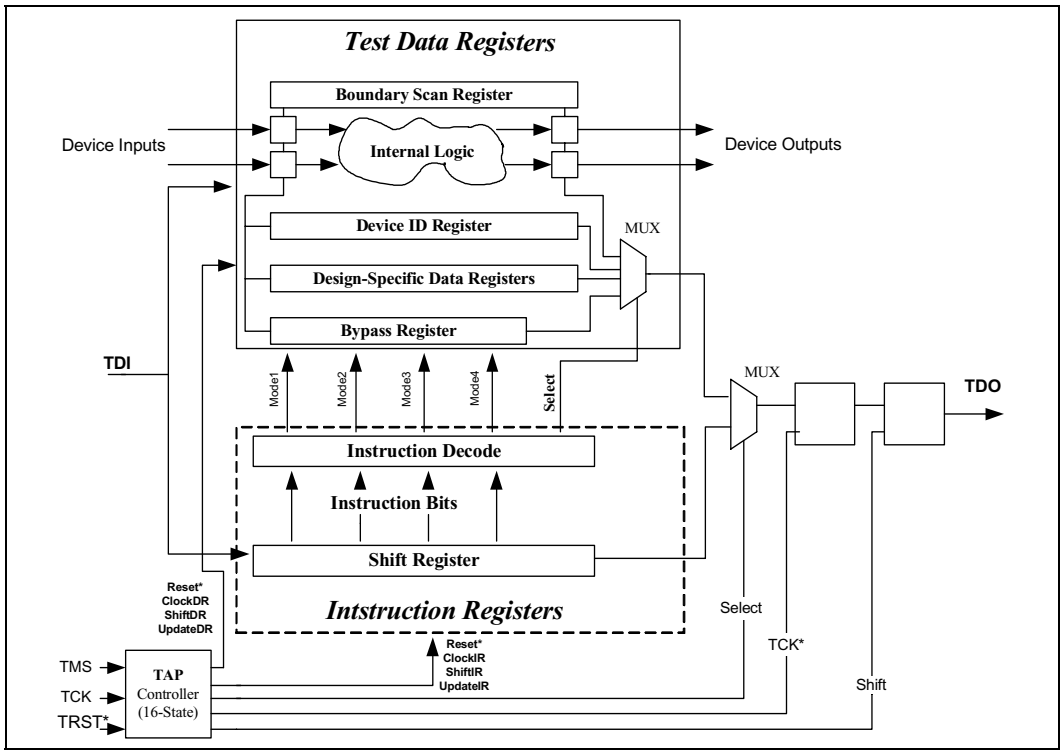
- five dedicated boundary scan pins.
- a state machine called the TAP.
- decode data registers.
- an instruction register.

The 31154 bridge contains test logic that is compatible with the IEEE Standard 1149.1-1990 Test Access Port (TAP) and Boundary Scan Architecture. Logic that conforms to this standard contains the following:

1. A Test Access Port (TAP) + five control pins (TDI, TMS, TRST#, TDO, and TCLK).
2. A TAP controller.
3. An instruction register.
4. A group of test data registers.

Each of these will be described in more detail later in this chapter. Figure 10 shows a generic diagram for logic conforming to the IEEE 1149.1 test standard.

Figure 10. IEEE 1149.1 Std. Block Diagram



7.1.1 Boundary Scan Pins and TAP Controller

The Test Access Port (TAP) Controller is a 16-state finite state machine, used to control the flow of data and instructions to and from the boundary scan circuitry. The TAP has five dedicated pin connections: TCK, TRST, TMS, TDI, and TDO. Transitions in the TAP controller only occur on the rising edge of the Test Clock (TCK), or upon the assertion of Test Reset (TRST). The Test Data Input and Output pins (TDI, TDO) are used shift data and instructions into the TAP and read results from the IC. In addition, the Test Mode signal (TMS) is used to control the transition of states within the TAP controller.

7.1.1.1 Test Clock (TCK)

This is the clock input for the test logic defined by this standard, i.e. the TAP controller and associated registers. The TLU is a fully static design, thus all registers retain their states indefinitely when TCK is stopped at “0” or “1”.

7.1.1.2 Test Mode Select (TMS)

This pin is used to control the operation of the TAP controller. The signal received at TMS is decoded by the TAP controller to control test operations. The state of TMS is sampled on the rising edge of TCK. Internally, there is a weak pull-up on this pin to provide a logic high when not driven, per standard definition.

7.1.1.3 Test Data Input (TDI)

This pin is used to provide serial input data to the instruction and test data registers. Data at TDI is sampled on the rising edge of TCK. Data shifted from TDI through a register to TDO appears non-inverted at TDO after a number of rising and falling edges of TCK determined by the length of the instruction or test data register selected. Internally, there is a weak pull-up on this pin to provide a logic high when not driven, per standard definition.

7.1.1.4 Test Data Output (TDO)

This is the serial data output pin. Changes in the state of TDO occur only following the falling edge of TCK while performing a shift operation. This pin is only driven while scanning (in SHDR or SHIR states) otherwise it is in inactive (high Z) state. The non-shift inactive state is provided to support parallel connection of TDO outputs at the board or module level.

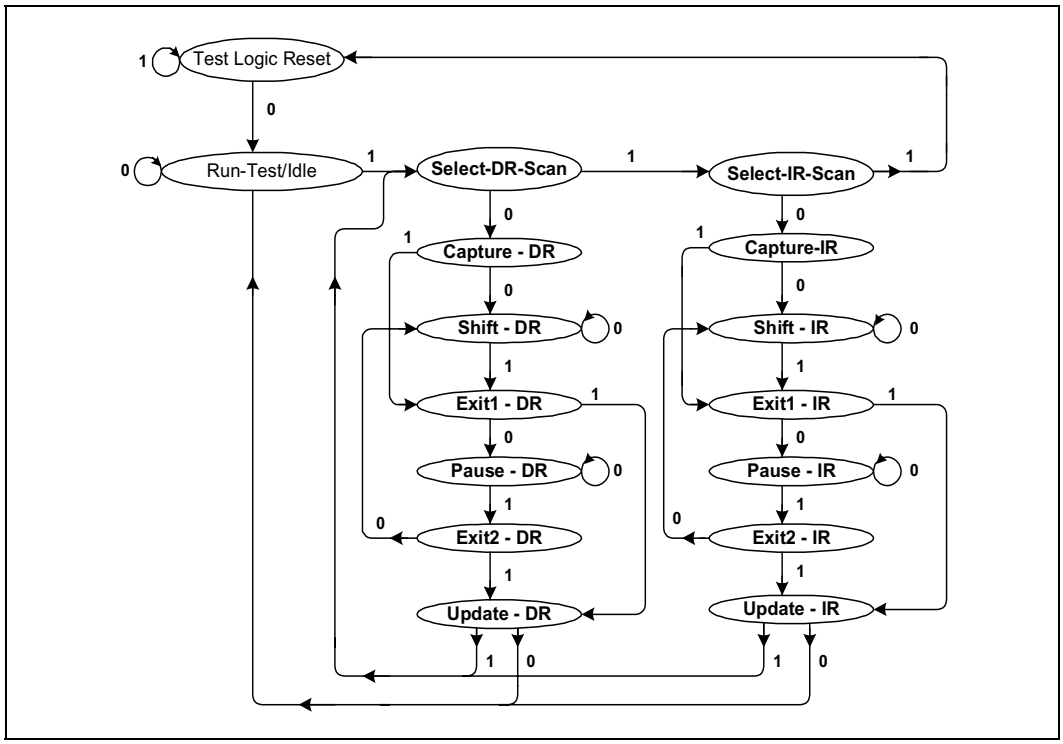
7.1.1.5 Asynchronous Reset (TRST#)

The TRST# signal is used to asynchronously reset the TAP controller and boundary-scan registers. The TAP controller is not initialized by any other system input, including system reset. The TAP controller initializes asynchronously on the falling edge of TRST# to the Test-Logic_Reset (initial) state. Upon reset, the TAP instruction register initializes to 0100 (IDCODE instruction). Internally, there is a weak pull-up on this pin to provide a logic high when not driven.

7.1.2 TAP Controller State Machine

The TAP controller, shown in Figure 11, is a sixteen-state synchronous finite state machine that changes state on the rising edge of TCK. The controller's next state is controlled by the state present at the TMS input. The TAP controller generates control signals, which together with TCK and control signals decoded from the instruction active in the instruction register, determine the operation of the test circuitry as defined by the IEEE Standard.

Figure 11. Tap Controller State Machine



7.1.2.1 Test-Logic-Reset

Test-Logic-Reset is the reset state. Boundary Scan test logic is disabled and the device IC operate in normal mode.

Transition to next state: On the rising edge of TCK **(1)** if TMS goes low one cycle, move to Run-Test/Idle **(2)** if TMS remains high, stay in Reset.

7.1.2.2 Run-Test/Idle

Run-Test/Idle is an idle state where activity previous instructions can play out. While in this state, activity in selected test logic occurs only if certain instructions (e.g. RUNBIST) are present.

Transition to next state: On the rising edge of TCK **(1)** if TMS goes high one cycle move to Select-DR-Scan. **(2)** If TMS remains low, stay in Idle.

7.1.2.3 Select-xx-SCAN (DR or IR)

Select-xx-SCAN is a temp controller state. Here the decision is made to enter the Data register column, the Instruction register column, or return to the Test- Logic-Reset.

Transition to next state: On the rising edge of TCK **(1)** At Select-DR, if TMS goes low move to Capture-DR, else move to Select-IR. **(2)** At Select-IR, if TMS goes low move to Capture-IR, else move to Test-Logic-Reset.

7.1.2.4 Capture (IR and DR)

IR: The shift register (within the Instruction Register) parallel loads a pattern of fixed logic values on the rising edge of TCK.

DR: Allows data to be parallel loaded into the Test Data Registers selected by the current instruction on the rising edge of TCK.

Transition to next state: On the rising edge of TCK **(1)** At Capture-IR, if TMS goes low move to Shift-IR, else move to Exit1-IR. **(2)** At Capture-DR, if TMS goes low move to Shift-DR, else move to Exit1-DR.

7.1.2.5 Shift (IR and DR)

IR: The shift register contained in the instruction register is connected between TDI and TDO, shifting data one stage towards its serial output on each rising edge of TCK.

DR: This Test Data Register, i.e. Boundary Scan, Bypass, Device ID, connected between the TDO and TDI (as a result of the current instruction) shifts data one stage towards its serial output on each rising edge of TCK.

Transition to next state: On the rising edge of TCK **(1)** At Shift-IR, if TMS goes high move to Exit1-IR, else remain at Shift-IR. **(2)** At Shift-DR, if TMS goes high move to Exit1-DR, else remain at Shift-DR.

7.1.2.6 Exit1 (IR and DR)

Exit1 is a temporary controller state. It is consistent between IR and DR.

Transition to next state: If TMS is held high during the next rising edge of TCK, transition to the Update state occurs, which terminates the scanning process. If TMS is held low during the next rising edge of TCK, the controller enters the Pause state.

7.1.2.7 Pause (IR and DR)

Pause is a state that allows a pause in the shifting of the instruction register (Pause-IR) or the test data register in the serial path between TDI and TDO (Pause-DR).

Transition to next state: On the rising edge of TCK, if TMS remains low, the controller remains in the pause state. When TMS goes high, the controller moves to Exit2.

7.1.2.8 Exit2 (IR and DR)

Exit2 is a temporary controller state. It is consistent between IR and DR.

Transition to next state: If TMS is held high during the next rising edge of TCK, transition to the Update state occurs, which terminates the scanning process. If TMS is held low during the next rising edge of TCK, the controller re-enters the Shift state.

7.1.2.9 Update (IR and DR)

IR: The instruction that was shifted into the instruction register is latched onto the parallel output from the shift-register path, on the falling edge of TCK. Once latched, it becomes the current instruction.

DR: Data is latched into the parallel output of shift registers from the shift register path, on the falling edge of TCK.

Transition to next state: On the rising edge of TCK, if TMS remains high then the controller moves to the Select state, else the controller moves to the Run-Test/Idle state.

The state registers and logic for this state machine can be seen in the IEEE Standard Test Access Port and Boundary-Scan Architecture Spec., section 5.2.2. The only inputs from outside the FUB are: TCK, TMS, TDI, TRST*.

7.1.3 Instruction Register

The 31154 Bridge TAP controller contains an instruction register (IR). The R is a 7-bit, parallel-loadable, serial-shift register with latched outputs. It used to select the test data register to be accessed, the test to be performed, or both.

When the TAP controller is in the Shift-IR state, instructions are loaded serially via TDI clocked by the rising edge of TCK. The shifted-in instruction becomes active upon latching from the master-stages to the slave-stages in the Update-IR state. At that time the IR outputs, along with the TAP finite state machine outputs, are decoded to select and control the test data register selected by that instruction. Upon latching, all actions caused by any previous instructions must terminate.

On activation of TRST#, the latched instruction will asynchronously change to the IDCODE (0100) instruction. Additionally, upon entering the Test-Logic-Reset state, the IDCODE instruction is latched and becomes active on the falling edge of TCK.

7.1.3.1 Instructions

The TAP controller instruction set is composed of both public and private instructions. Public instructions are intended for use by purchasers of the part. Private instructions are intended solely for the use of the manufacturer.

Since the instruction set for each TAP controllers is independent of one another, each is listed in Table 104 below.

Table 104. TLU TAP Controller Instruction Set

Instruction	Opcode	Public/Private	Description
EXTEST	0000	Public	Intended for supporting the boundary-scan feature for testing device interconnects at the board/system level, the EXTEST instruction will connect only the boundary-scan register between TDI and TDO in the Shift-DR state. When EXTEST is selected, all output signal pin values are driven by values shifted into the boundary-scan register and may change only on the falling-edge of TCK in the Update_DR state. Also, when extest is selected, all system input pin states must be loaded into the boundary-scan register on the rising-edge of TCK in the Capture_DR state. Note: Data would typically be loaded onto the latched parallel outputs of boundary-scan shift registers using the SAMPLE/PRELOAD instruction prior to selection of the EXTEST instruction.
SAMPLE/ PRELOAD	0001	Public	SAMPLE/PRELOAD performs two functions: • When the TAP controller is in the Capture-DR state, the sample instruction occurs on the rising edge of TCK and provides a snapshot of the component's normal operation without interfering with that normal operation. The instruction causes Boundary-Scan register cells associated with outputs to sample the value being driven by or to the processor. • When the TAP controller is in the Update-DR state, the preload instruction occurs on the falling edge of TCK. This instruction causes the transfer of data held in the boundary-scan cells to the slave register cells. Typically the slave latched data is then applied to the system outputs by means of the extest instruction.
HighZ	0011	Public	HIGHZ puts all output pins into a tri-state mode. The clocks are not stopped. When this instruction is active, the bypass register is connected between TDI and TDO.
IDCODE	0100	Public	IDCODE is used in conjunction with the device identification register. When selected, IDCODE parallel-loads the hard-wired identification code (32 bits) into the identification register on the rising edge of TCK following entry into the Capture-DR state. The instruction selects only the identification register for connection between TDI and TDO in the Shift-DR state for serial access. NOTE: The device identification register is not altered by data being shifted in on TDI.
CLAMP	0101	Public	Once the clamp instruction is loaded into the TAP controller instruction register, the output pins are driven by the parallel output of the boundary-scan chain. The bypass register is selected as the serial path between TDI and TDO when the TAP controller passes through the Shift-DR state.
BYPASS	1111111_2	Public	BYPASS selects the bypass register between TDI and TDO while in Shift-DR state, effectively bypassing the processor's test logic, '0' is captured in the Capture-DR state. While this instruction is in effect, all other test data registers have no effect on the operation of the system.

7.1.4 Data Registers

The Data Registers in JTAG are used to access areas of the device for the purpose of controllability, observability, or both. Each named test data register has a fixed length and can be accessed using one or more instructions. Further description can be found in the IEEE Std, 1149,1-1990, Chapter 8.

7.1.4.1 Boundary Register

This register is a collection of cells laid out around the perimeter of the system logic of the 31154 Bridge, forming a single shift register between TDI and TDO. Each cell of the Boundary-Scan Register is matched with an existing output buffer of a system pin. Further definition, rules, and specifics of the Boundary-Scan Register can be found in the IEEE Std, 1149,1-1990, Chapter 10.

7.1.4.2 Device ID Register

This register allows the manufacturer, part number, and version of a component to be determined through the TAP. This circuitry (register cells) is a dedicated part of the test logic and is not usable during system functionality. Further definition, rules, and specifics of the Device ID Register can be found in the IEEE Std, 1149,1-1990, Chapter 11.

7.1.4.3 Bypass Register

This register is used to “bypass” all other test data registers, providing a serial path for shifting data directly from TDI to TDO. This register is used during board-level test operation. Further definition, rules, and specifics of the Bypass Register can be found in the IEEE Std, 1149,1-1990, Chapter 9.